# EPITAXIAL GRAPHENE FILMS ON SIC: GROWTH, CHARACTERIZATION, AND DEVICES

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# EPITAXIAL GRAPHENE FILMS ON SIC: GROWTH, CHARACTERIZATION, AND DEVICES

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*To my wife, Qinyi and my daughter, Kathleen*

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# SUMMARY

Carriers in graphene (a single sheet of graphite) are massless Dirac fermions that have excellent transport properties, such as high mobility, long phase coherence length, suppression of the backward scattering, etc. Epitaxial graphene on SiC provides a promising 2D platform for graphene-based electronic devices that can be integrated into IC technology.

Large scale, high quality epitaxial graphene films are grown on the SiC substrates in an homemade induction vacuum furnace by thermal decomposition of SiC at high temperatures. Graphene films continuously grow over the terraces of the whole SiC surface. Epitaxial graphene films have been characterized comprehensively by tools of atomic force microscopy (AFM), scanning electron microscopy (SEM), scanning tunneling microscopy (STM), high resolution transmission electron microscopy (HRTEM), low energy electron diffraction (LEED), Auger electron spectroscopy (AES), X-ray scattering, micro-Raman spectroscopy, etc. Epitaxial Graphene films are highly ordered and extremely flat on both polar faces (Si face and C face) of SiC. The relative rotations between graphene layers make epitaxial graphene on the C face different from Bernal graphite that is AB stacked between adjacent graphene layers.

Carriers in epitaxial graphene act as massless Dirac fermions in single graphene sheet, which is demonstrated by infrared Landau level spectroscopy experiments and magneto-transport measurements. Dirac properties of carriers in epitaxial graphene include the linear square root B dependence of energy, anomalous Berry's phase $\pi$, weak anti-localization, etc. Carriers in epitaxial graphene also show a long phase coherence length ($\sim \mu$m), a high mobility of above $10^4 cm^2/Vs$. Quantum confinement due to the width restriction is observed on an epitaxial graphene ribbon. The electric field effect on epitaxial graphene is realized in both top gated and side gated field effect transistors (FETs). All these evidences demonstrate the great potential of epitaxial graphene in future electronic applications.

# CHAPTER I

# INTRODUCTION

Graphene is a single sheet of graphite. While bulk graphite is semimetal, graphene is a zero bandgap semiconductor. Band structure calculations show graphene has a linear energy dispersion relation in the low energy region close to the Dirac points where the conduction band and the valence band touch. Carriers in graphene are described as massless Dirac fermions in contrast to massive carriers in normal metals and semiconductors that obey a parabolic energy dispersion relation. The uniqueness of graphene band structure indicates its peculiar electronic transport properties.

Although graphene theory has been applied to study layer materials and carbon based materials such as carbon nanotubes (CNTs), the first observation of graphene on an insulating substrate was realized in late 2004 when graphene flakes peeled from bulk graphite were identified under a phase contrast microscope with a 300nm $SiO_2$ layer as reference. Since then, many groups have explored physical and electronic properties, especially transport properties in graphene or few-layer graphene (FLG). Some important new phenomena have been observed in the past four years, including anomalous quantum Hall effect, anomalous Berry's phase, conductivity minimal, high field degeneracy splitting, suppression of weak localization, long phase coherence length, quantum confinement, etc [17, 19, 40, 153, 156, 237, 251, 252, 254].

Epitaxial graphene has been studied in our group since 2001. In our studies, high quality, large scale epitaxial graphene films are grown on SiC substrates. Our final goal is to develop a process scalable to industrial applications. Therefore we have chosen a fundamentally different approach from the method of mechanical exfoliation from bulk graphite. Initially, the concept of epitaxial graphene was motivated by the predicted physical similarities between graphene and CNTs. Even although CNTs have been extensively studied for nearly two decades, CNTs are limited for real device applications due to several critical

problems such as CNT chirality control during growth, large contact resistance with metal electrodes, and limited integration possibilities with standard Si technology. Graphene ribbons can be viewed as unrolled CNTs. Calculations show that graphene ribbons should preserve the essential properties of CNTs such as ballistic transport, geometry dependence, electronic structure, and gating capability. The advantage of epitaxial graphene is that it is a 2D platform compatible with standard semiconductor processing.

In this thesis work, the hexagonal 4H-SiC and 6H-SiC are chosen as substrates for epitaxial graphene growth. 4H-SiC and 6H-SiC have two polar faces: the (0001) Si terminated face and the $(000\bar{1})$ C terminated face. Single and multi-layer graphene films can grow on either the Si face or the C face in a homemade induction vacuum chamber by thermal decomposition of SiC at high temperatures. The surface morphology and crystal structure of epitaxial graphene are studied with atomic force microscope (AFM), low energy electron diffraction (LEED), Auger electron spectroscopy (AES), X-ray reflectivity, high resolution transmission electron microscopy (HRTEM), and scanning electron microscopy (SEM), etc. The transport properties of epitaxial graphene are studied in magneto-transport experiments in a wide temperature range. Moreover an epitaxial graphene film turns out to be a multilayered graphene because the carriers in epitaxial graphene act as those in single graphene sheet. Epitaxial graphene top gated and side gated field effect transistors (FETs) have also been successfully fabricated. These systematic studies unambiguously demonstrate the high quality of epitaxial graphene on SiC and the great potential of epitaxial graphene for electronic applications.

Chapter II and III briefly review the theory and applications of graphite and graphene, respectively. Comparing graphite with graphene gives us a better understanding why graphene is different from graphite. Chapter IV introduces the crystal structures and properties of SiC polytypes, and explains why hexagonal 4H- and 6H- SiC are chosen as substrates for epitaxial graphene growth. SiC bulk and epitaxial growth are described to obtain a better understanding of the complexity of SiC graphitization. Chapter V describes the hydrogen etching treatment on SiC substrates to achieve atomic flat SiC surfaces for the following epitaxial graphene film growth. Chapter VI describes the growth of epitaxial

graphene on SiC substrates in a homemade induction vacuum chamber, and demonstrates the high crystal quality of epitaxial graphene as analyzed by AFM, LEED, AES, HRTEM, and X-ray reflectivity. Based on X-ray reflectivity experiments, an epitaxial graphene-SiC interface model is given to explain why multilayer epitaxial graphene behaves as a single graphene sheet. Chapter VII presents the potential of epitaxial graphene for device fabrication. Standard lithography tools and semiconductor processing techniques are described briefly. Finally, Chapter VIII discusses important transport phenomena observed in epitaxial graphene, and demonstrates epitaxial graphene can be gated by an external electric field.

# CHAPTER II

# INTRODUCTION TO GRAPHITE

Graphene is a single sheet of graphite. Graphite consists of identical graphene layers that are stacked up in a certain periodic sequence. Graphite has been well studied in theory and in experiment in the past tens of years. Although graphene has been applied in theoretical calculation of bulk graphite, its experimental studies were not reported until late 2004. Different from bulk graphite, graphene owns many unique physical and electronic properties. From the view of history, it is necessary to first introduce graphite in aspects of its physical and electronic properties for a better understanding of graphene. This chapter briefly reviews the band structure of graphite and its transport properties.

## *2.1 Crystal Structure of Bulk Graphite*

Figure 2.1 shows the crystal lattice structure of graphite. Graphite is a lamellar material, consisting of stacked graphene layers. The carbon atoms in a graphene layer are covalently bound to form a hexagonal two-dimensional array. In a graphene layer, the carbon-carbon distance is 1.42Å. So that the lattice constant is 2.46Å. The van der Waals force causes the adhesion of adjacent graphene layers. The spacing between adjacent layers is 3.35Å [37].

Graphene layers can be stacked in different sequences. Both Bernal graphite( with AB stacking sequence) and rhomboheral graphite (with ABCBC stacking sequence) occur naturally. The stacking sequences of these two kinds of graphite are illustrated in Figure 2.2 [30]. In a Bernal structure, carbon atoms in the layer B are directly above the center of a carbon hexagon in the layer A. In a rhomboheral structure, the center of a carbon hexagon in the layer A is directly below a corner of a hexagon in the layer B, which is in turn directly below an nonequivalent corner of a hexagon in the layer C [37]. As discussed later, different stacking sequences affect the band structure and properties of graphite.

Graphite can be obtained from different sources [43]. Large single crystal Bernal stacked graphite is scarce in nature. It is not convenient for physical property measurements because

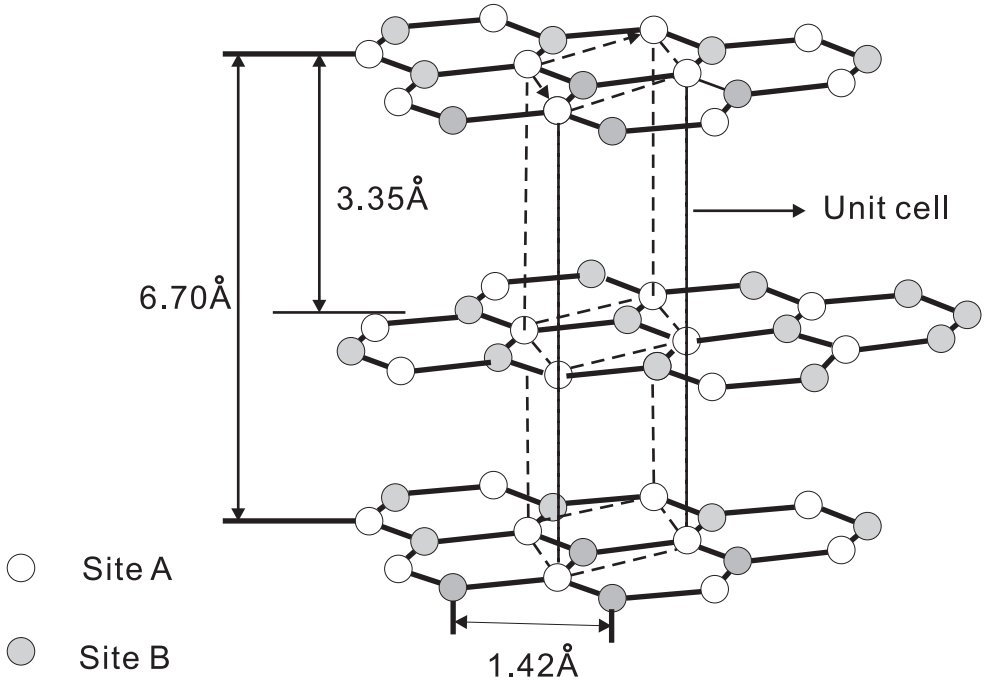


**Figure 2.1:** Crystal lattice structure of graphite (Bernal).

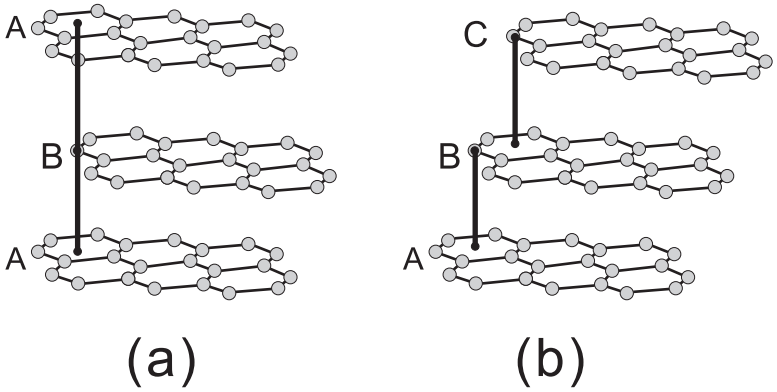


**Figure 2.2:** The stacking sequences of three graphite structures. (a) Bernal(ABAB); (b) rhomboheral (ABCABC).

of the high defect density, inclusions, and stacking faults. Another kind of Bernal stacked graphite is kish graphite, obtained by the carbon crystallization from molten steel in the steel manufacturing process. Kish graphite samples typically contain several large single crystallites. Highly oriented pyrolytic graphite (HOPG) is a synthetic graphite formed by cracking a hydrocarbon at high temperatures and a subsequent high pressure heat treatment [157]. HOPG is highly oriented along c-axis and consists of ordered monocrystal graphite grains. The grains are micrometers in size and they are slightly disoriented with respect to each other. The term mosaic spread is used to characterize the perfection of HOPG samples. A more ordered HOPG has a smaller mosaic spread.

## *2.2 Band Structure of Bulk Graphite*

Because the van der Waals force between adjacent layers in graphite is weak, the first band structure calculations neglected the interlayer interaction in graphite. Hence graphene was actually proposed as an approximate model for graphite [200]. In fact, the difference between graphite and graphene is caused by the weak interlayer interaction. While the band structure of graphene has a zero bandgap, three dimensional graphite has a band overlap. The band overlap produces the semimetallic properties of graphite with electrons and holes.

I next discuss Bernal graphite in detail. A number of band structure calculations of three dimensional graphite have been proposed in the past decades [30, 37, 124, 215]. The Slonczewski-Weiss-McClure (SWMcC) band model was developed by Slonczewski and Weiss (1958) and McClure (1957, 1960) to calculate the electronic structure of graphite near the Fermi level. In this model, the energy eigenvalues near the Fermi level are given as functions of several parameters that represent the orbital interactions of carbon atoms within the same plane and in the neighboring planes [37, 43]. This model is simple and often used to explain transport and optical properties of graphite near the Fermi level [5].

In the crystal structure of graphite, there are two inequivalent atomic sites: A and B (see Figure 2.1). Carbon atoms at site A have neighbors directly above and below in adjacent layers, and carbon atoms at site B do not. The unit cell of graphite contains four atoms as seen in Figure 2.1. The Brillouin zone of the reciprocal lattice is shown in Figure 2.3. The

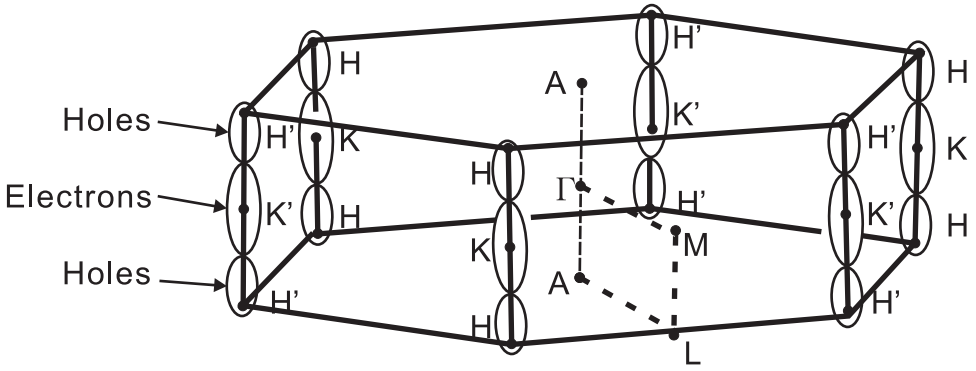


**Figure 2.3:** Graphite Brillouin zone with several high symmetry points. Electron and hole Fermi surfaces are located along the edges of HKH and H'K'H' [43].

electronic energy bands near the HK axis in the three-dimensional graphite are shown in Figure 2.4.

Since each carbon atom has four valence electrons, there are totally 16 energy bands (excluding spin), 12 $\sigma$ bands and 4 $\pi$ bands. The energies of the $\pi$ bands are within the 6 antibonding $\sigma$ bands and 6 bonding $\sigma$ bands. Two $\pi$ bands are antibonding and two $\pi$ bands are bonding. Along the Brillouin edges of HKH and H'K'H', these four $\pi$ bands are labeled $E_1, E_2$, and $E_3$ (doubly degenerate). The $E_1$ band is empty. The $E_2$ band is nearly full and defines the minority hole packet near the zone corner. The $E_3$ band is along the zone edge and lies close to the Fermi level. The $E_3$ band is partly occupied and defines the majority electron and hole pockets. The Fermi level is chosen so that the volume of electron pocket are equal to that of hole pocket. The interlayer interaction has a profound effect on the four $\pi$ bands near the Brillouin zone edges, causing a band overlap of about 40 meV [43, 85].

Other methods [5, 215] also have been carried out to calculate the three dimensional band structure of graphite. These methods yield good agreement with the SWMcC model.

The effect of different stacking sequence of graphite layers (AAA, ABAB, and ABCABC) on the electronic structure of graphite has been evaluated by different models [30, 68, 125]. The Haering-McClure model [68] was used to calculate the band structure of rhombohedral graphite. Charlier, et al., extended the SWCMcC model to calculate the band structure of AAA stacking near the Fermi energy, and compared the energy difference near the Fermi

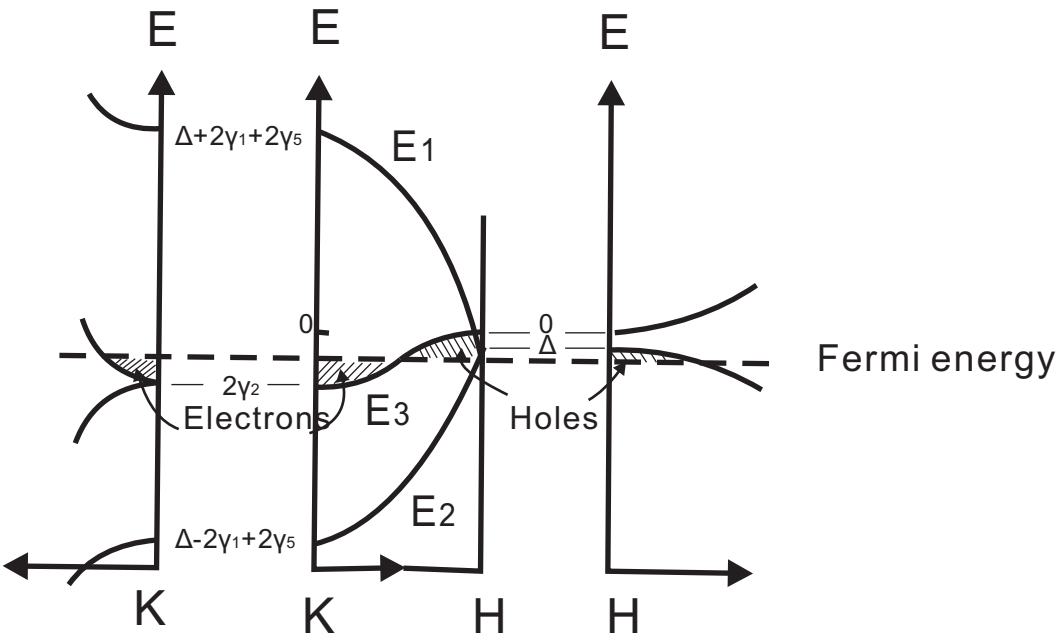


**Figure 2.4:** Electronic energy bands near the H-K-H axis in the three-dimensional graphite as obtained from the SWMcC band model. The $E_3$ band is doubly degenerate along the H-K-H axis (See center figure) and is lifted when away from the H-K-H axis (See left-hand and right-hand figures.) [43].

level among these three types of stacking. They show that different stacking arrangements lead to a nearly identical band structure except for the region near the Fermi level [30].

The low energy region near the Fermi surface of graphite has been studied by magnetoresistance, magnetoreflectance, cyclotron resonance, magnetic susceptibility, and other techniques [44, 162, 215]. The higher energy region of band structure has been measured using photoemission, secondary electron emission, electron spectroscopy, and electron energy loss spectroscopy [43]. The effect of external pressure on the Fermi surface of graphite was also studied in theory and experiment [5, 9].

### *2.3 Transport Properties of Bulk Graphite*

Because of the weak interlayer interaction, carrier transport in graphite is essentially two dimensional. Graphite shows a large electrical anisotropy with a high in-plane conductivity $\sigma_a \sim 10^4 \Omega^{-1} cm^{-1}$and a low c-axis conductivity $\sigma_c \sim 10 \Omega^{-1} cm^{-1}$ [43]. A higher $\sigma_a/\sigma_c$ ratio indicates a higher quality graphite. Graphite also has high in-plane mobilities of $\sim 10^4 cm^2/Vs$ at room temperature and $\sim 10^5 - 10^6 cm^2/Vs$ at 4 K [43, 205]. Due to the

electron-hole compensation near the Fermi level, graphite has a low free carrier concentration of $\sim 10^{-4}$ per atom at room temperature [43].

The temperature dependence of graphite conductivity is dominated by changes of the total carrier density and mobility with temperature. Graphite has three types of free carriers: majority electrons, majority holes, and minority holes (see Figure 2.4). The total carrier density decreases with decreasing temperature. Because electron-phonon scattering also diminishes upon cooling, the in-plane mobility of graphite increases with decreasing temperature. Consequently, the in-plane conductivity of graphite of high quality only mildly increases with decreasing temperature. At 4 K, graphite has a typical relaxation time $\tau \sim 10^{-11}$s and mean free path $l \sim \mu m$ [43]. The temperature dependence of the c-axis conductivity is very weak since temperature-independent defect scattering determines the conduction along c-axis.

The electrical conductivity, Hall coefficient, magnetoresistance, and other transport properties have been extensively studied from classical transport region to quantum transport regime [21, 88, 115, 116, 126, 162, 206, 208, 234]. The carrier density can be measured by various methods. The most sensitive method is to determine the Fermi surface cross sectional areas and k-space volumes in each carrier pocket by quantum methods such as Shubnikov-de Haas oscillations and de Haas-van Alphen oscillations [14, 43].

The Hall coefficient is very small in graphite due to the compensation of electron and hole carriers that have similar densities and mobilities. The small remaining density inequality between electrons and holes leads to a complicated dependence on temperature and magnetic field.

The magnetoresistance behavior of graphite has been studied from low to high magnetic fields. In low magnetic fields, the magnetoresistance of graphite exhibits a quadratic field dependence [162, 207, 234]. In a high magnetic field, carriers occupy discrete Landau levels. Different methods are utilized to study quantum oscillations in graphite in high magnetic fields at low temperatures [21, 123, 208, 234]. In a higher magnetic field ($\geq$ 7.3 T), the quantum limit is reached and carriers only occupy the lowest Laudau level of graphite [236]. A huge linear magnetic field dependence of the magnetoresistance was observed. Possible

mechanisms were proposed to explain this linear dependence [2, 3, 43, 87, 126]. Above 12 T, the magnetoresistance starts to saturate [85]. The saturation phenomenon was explained by the freeze-out effect of the ionized impurity scattering centers [211]. In the extreme high magnetic field ($\geq$ 20 T) [85], a high-field anomaly in the magnetoresistance was found and suggested to be an electronic phase transition involving many-body effects. Yoshika and Fukuma proposed a model which ascribed this sharp resistance increase to a charge-density-wave (CDW) instability caused by Landau quantization [249]. Their model was confirmed by the observation of reentrant transition from field-induced density wave state to the normal state in large magnetic fields ($\sim$ 50 T) [242].

## *2.4 Summary*

Due to the weak interlayer interaction, graphite is semimetallic with both electron and hole carriers at the Fermi level. Different stacking sequences (ABABAB, and ABCABC) of planes give two kinds of graphite: Bernal and rhomboheral. These two kinds of graphite have similar band structures except for the regions close to the Fermi level. Graphite shows complicated transport properties concerning carrier density, mobility, conductivity anisotropy, temperature dependence, and magnetic field dependence.

# CHAPTER III

# GRAPHENE: THEORY AND POSSIBLE APPLICATIONS

In 2001 our group started to pursue large-scale high-quality epitaxial graphene films on SiC and expect that the excellent transport properties of CNTs would be reflected in graphene. More than that, graphene provides a 2D platform to easily integrate with Si technology. In 2004 and parallel to our work, other groups pursued a different approach to obtain graphene by mechanical exfoliation of bulk graphite. Since then, many interesting properties of graphene have been explored in experiment and in theory.

## *3.1 Band Structure of Graphene*

The band structures of graphene and few-layer graphene (FLG) have been studied by many groups using various models [10, 30, 64, 65, 83, 105, 113, 148, 170, 181]. Among the methods, the tight-binding (TB) method is the simplest and nevertheless gives reasonable results. This method focuses on the hopping of $\pi$ electrons from one carbon atom to its neighbors. The $\pi$ bands determine the transport properties in the low energy region near the K point (see Figure 3.3). The remaining $\sigma$ bands are far away from the K point such that their contribution to transport can be neglected.

### 3.1.1 Single-layer Graphene

In graphene, the unit cell contains two inequivalent carbon atoms: A, B as shown in Figure 3.1(a). $\mathbf{a}_1$ and $\mathbf{a}_2$ are the lattice vectors, where a is the lattice constant a=2.46Å.

$$\mathbf{a}_1 = \left(\sqrt{3}a/2, a/2\right), \mathbf{a}_2 = \left(\sqrt{3}a/2, -a/2\right)$$

Figure 3.1(b) shows the reciprocal lattice that also has hexagonal symmetry. The primitive lattice vectors $\mathbf{b}_1$ and $\mathbf{b}_2$ are calculated by the relationships,

$$\mathbf{b}_1 = 2\pi \frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}, \mathbf{b}_2 = 2\pi \frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}$$

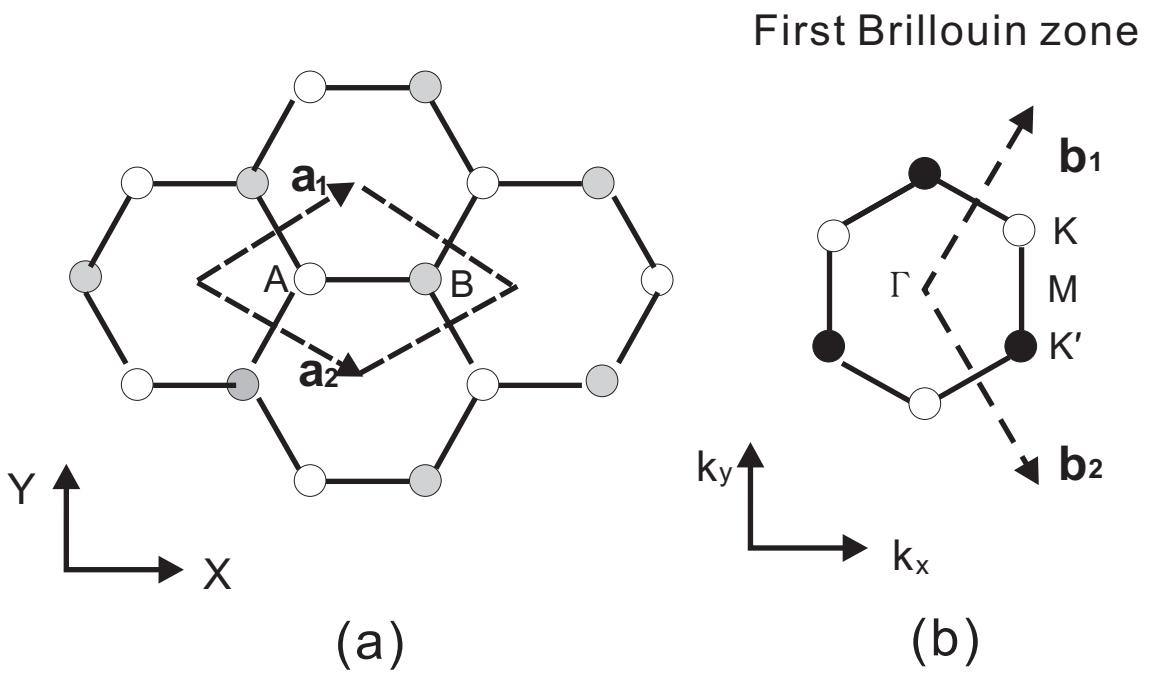


**Figure 3.1:** (a) Graphene hexagonal lattice. $\mathbf{a}_1$ and $\mathbf{a}_2$ are the lattice vectors. (b) Sketch of the first Brillouin zone in the reciprocal lattice.

$\mathbf{a}_3$ is the unit vector along the c-axis. Hence,

$$\mathbf{b}_1 = \left(2\pi/\sqrt{3}a, 2\pi/a\right), \mathbf{b}_2 = \left(2\pi/\sqrt{3}a, -2\pi/a\right)$$

Wallace gave the first tight-binding description of graphene in 1947 [232]. He considered the nearest- and next nearest- neighbor interaction between $p_z$ orbitals with the neglect of the overlap between the wave functions from more remote atoms. Later Reich, et al., extended the interaction up to the third-nearest neighbors, and described the entire Brillouin zone. Their calculations had a good agreement with the first-principle results [181]. Below, the dispersion relation of graphene is given from a simple nearest-neighbor tight-binding calculation.

$$E\left(k_x, k_y\right) = \pm\gamma\sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)} \tag{3.1}$$

$\gamma$ is the nearest-neighbor hopping energy. $\gamma = 2.7$ eV.

Figure 3.2 shows the band structure of graphene according to Equation 3.1. In graphene, each unit cell contains two inequivalent carbon atoms. A free carbon atom has an electronic

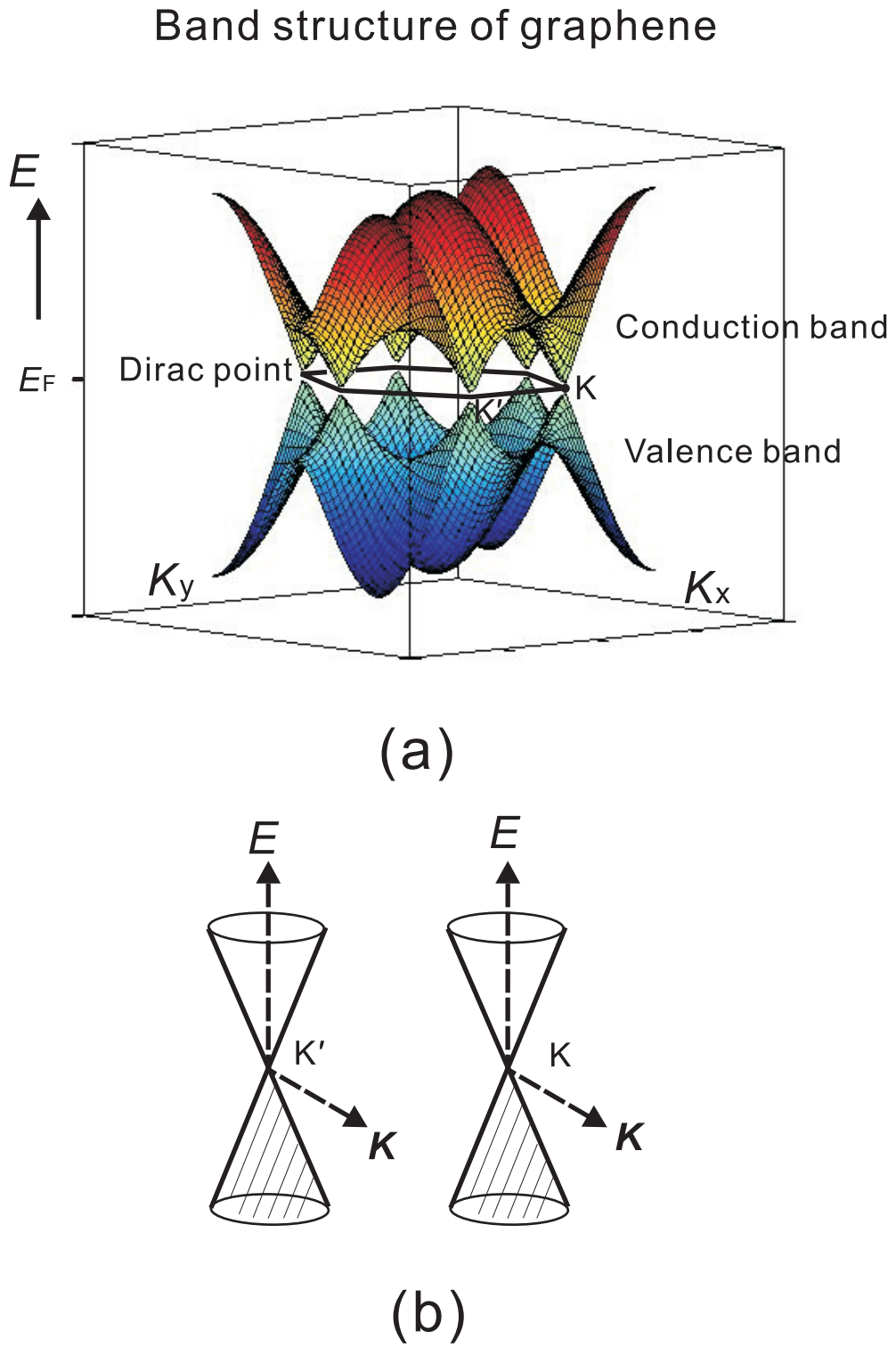


**Figure 3.2:** Band structure of graphene. (a) The energy of the conduction band and the valence band as a function of wavevector $\boldsymbol{K}$. (b) The energy dispersion relation near the Dirac points (K, K').

configuration of $1s^2 2s^2 2p^2$. Without the interlayer interaction, the intraplanar interaction between the $2s$, $2p_x$, $2p_y$ atomic orbitals forms the strongly coupled bonding and antibonding trigonal orbitals, which gives rise to three bonding and three antibonding $\sigma$ bands. The weakly coupled $2p_z$ gives rise to two $\pi$ bands. The $\pi$ bands are between the antibonding and bonding $\sigma$ bands. The lower $\pi$ bonding band forms the valence band, and the upper $\pi$ antibonding band forms the conduction band. The conduction band and valence band touch at precisely two kinds of inequivalent corners (K, K') of the first Brillouin zone of graphene. These two kinds of corners are called Dirac points (see Figure 3.2).

Carriers in graphene obey the Dirac-Weyl equation for the hamiltonian $H = \hbar V_F \cdot \sigma \cdot k$, where $V_F$ is the Fermi velocity, $\sigma$ is the 2D Pauli matrix, and $\hbar k$ is the momentum [57]. It leads to a massless dispersion relation of $E = \hbar V_F |k|$, with $V_F = \sqrt{3}a\gamma/2\hbar = 9 \times 10^5 m/s$, where the nearest C-C distance $a$=1.42 Å . The Fermi velocity is about 300 times slower than the light speed $c$ [238]. Figure 3.2(b) shows the linear energy dispersion relation near the Dirac points for $\pi$ bands. The linear dispersion relation results in a linear density of states near the Dirac points. The conduction and valence bands are degenerate by symmetry at K and K' where the Fermi level passes. The density of states at the Fermi level is zero, so graphene is a two valley (K and K') zero-gap semiconductor [43, 124, 37].

The Dirac-Weyl equation also introduces an additional quantum number label $\sigma$ (referred as pseudospin) due to the equivalence of A, B sublattices in the graphene honeycomb crystal lattice (see Figure 3.1). Pseudospin, like spin, has two values. But different from spin, pseudospin is coupled to the momentum in a chiral way. As discussed later, the chiral nature of carriers does not favor backward scattering in graphene.

### 3.1.2 Few-layer Graphene

For FLG systems, different stacking sequences affect their band structures. Several groups have calculated the low energy band structures of FLG, typically from bilayer (AB or AA stacked), trilayer (ABA or ABC stacked), to tetralayer (ABAB, ABCA, ABAC, and ABCB stacked) [10, 65, 113, 170].

It is found that AB-bilayer graphene is a zero gap semimetal with a parabolic dispersion

relation. When a perpendicular electric field is applied, the symmetry along the c-axis is broken and the two layers are no longer equivalent. Thus an energy gap of about 30 meV is induced between the conduction band and the valence band in an external electric field of 77.94 mV/Å[10]. ABA-trilayer graphene is semimetallic with a very small overlap between the conduction and valence bands. An external electric field does not induce a band gap on the ABA-trilayer. ABC-trilayer graphene is a zero-gap semiconductor (or zero band-overlap semimetal) with a band contact near the K point on the KM symmetry line. The ABC-trilayer opens a gap at the K point under an electric field. Tetralayers are all semimetallic at zero field and no band gaps are created by an external electric field [10, 65].

Partoens, et al., studied the band overlap transition from graphene to Bernal stacked graphite around the K point [170]. As mentioned before, graphite is a semimetal with a band overlap of about 40 meV. Bi-layer graphene is semimetal with a small band overlap of about 0.16 meV. For three or more layers, they are all semimetals and the band overlap increases with the number of layers. The band overlap difference between multi-graphene layers and bulk graphite is smaller than 10 % when there are more than 11 layers [170].

## *3.2 Ways to Obtain Graphene*

### 3.2.1 Mechanical Cleavage

In 1999, Prof. Rodney Ruoff's group at Northwestern University reported a method of rubbing tiny pillars of graphite against Si substrates to produce thin graphite disks [114]. His group also proposed to apply this method to achieve a single-layer graphene. Later Prof. Philip Kim's group at Columbia University took a similar approach of dragging a graphite crystal mounted to the AFM tip along a surface to separate graphite flakes from the bulk crystal. The separated flakes still contain at least 10 graphene layers [253]. The trick to this approach is finding and identifying the sparsely distributed single or few layer graphene flakes on the surface. In 2004, Prof. Andre Geim's group at the University of Manchester in England introduced the technique of micromechanical cleavage of bulk graphite with adhesive tape [154]. Geim's group used a phase-contrast optical microscope to identify single-layer graphene in the sea of bulk graphite. Graphene is generally invisible due to its

thinness. When placed on a Si wafer that is coated by a 300 nm thick thermal $SiO_2$ film, graphene becomes visible owing to the feeble interference-like contrast with respect to a bare wafer. From the tiny color change of $SiO_2$ layer on the Si wafer, single-layer graphene and FLG can be distinguished from bulk graphite. This optical method is very sensitive to the freshness of graphene, and the cleanness and the thickness of $SiO_2$. For example, a 5 % difference in $SiO_2$ thickness can make single-layer graphene completely invisible. Due to the low yield of graphene, patience and perseverance are required to find graphene [57].

Later other techniques have been applied to characterize the graphene quality and the layer number of FLG. These techniques include Raman spectroscopy, atomic force microscopy(AFM), electron diffraction, and transmission electron microscopy (TEM) [49, 129]. Among these techniques, Raman spectroscopy shows significant features sensitive to the layer number of FLG and is promising for an accurate thickness measurement [49, 61]. Electronic structures of graphene and FLG are different from each other due to the interlayer interaction modulation. The changes in the electron bands for single-, bi- and few-layer graphene can be reflected by Raman fingerprints. AFM has a thickness resolution up to 1 Å. But the interaction force between the substrate and graphene gives an uncontrollable distance between graphene and the substrate. Possible contaminants at the interface also affect the measurement of AFM. Thus the thickness measured by AFM sometimes leads to an incorrect estimation of the layer number of FLG. Suspended graphene sheets have been studied by electron diffraction and TEM [129]. TEM studies reveal suspended graphene sheets are not perfectly flat. According to the Mermin-Wager theorem, there should be no long-range order in two dimensions at any finite temperature [127]. Single-crystalline membranes can exist but should be rippled [90]. Meyer, et al., claim that suspended graphene sheets exhibit intrinsic microscopic ripple roughening, so that the surface's normal vector varies by several degrees, and out-of-plane deformations reach about 1 nm. Meyer, et al., also claim that the elastic corrugation on graphene sheets is consistent with the high mobility of charge carriers in graphene [133].

### 3.2.2 Epitaxial Graphene Growth on Silicon Carbide

Mechanical cleavage of bulk graphite provides a shortcut to study the physical and transport properties of single- or few-layer graphene. However, for electronic applications, single- or few-layer graphene has to be obtained by other, more efficient methods. Among them, epitaxial growth of high quality graphene on substrates offers the most viable approach toward this goal. Single- and multi- layer graphene films have been epitaxially grown on silicon carbide (typically on 4H- and 6H-SiC) by thermal decomposition of SiC at high temperature in ultrahigh vacuum (UHV) [17, 19, 31, 51]. Motivated by many resemblances of electronic properties of graphene and CNTs, our group as early as 2001 started to develop this epitaxial growth method to achieve high quality multilayer graphene in a home-made high vacuum graphite furnace. Epitaxial multilayer graphene films have been extensively characterized by surface analysis tools, electronic transport experiments, infrared spectroscopy, and other techniques [17, 18, 19, 40, 75, 76, 183, 186, 187, 237].

## *3.3 Transport Properties of Graphene*

Because of the linear energy dispersion near Dirac points at low energy excitations, massless fermion particles in graphene behave differently from other massive carriers with a parabolic dispersion relation in normal metals and semiconductors. In the past three years from 2004-2007, transport experiments have been reported on graphene obtained by mechanical exfoliation from several groups. Several unusual transport properties on exfoliated graphene are listed below.

- Anomalous quantum Hall effect in single-layer graphene,
- Anomalous quantum Hall effect in bi-layer graphene,
- Minimal conductivity,
- High field degeneracy splitting, and
- Suppression of weak localization.

Below, these properties are reviewed through a combination of experimental results and theoretical calculations.

In a typical transport experiment on exfoliated graphene, graphene layers are mechanically peeled from bulk graphite, and spun on a clean thermal $SiO_2$ layer of 300 nm thick on a degenerately doped Si wafer. Graphene flakes are randomly spotted by a combination of optical microscope, AFM, and Raman spectroscopy. The selected graphene flakes are further patterned into multi-terminal regular structures (such as Hall bars) by semiconductor processing techniques. The back gate voltage $V_g$ is added on the bulk Si wafer to tune the type and density of carriers in graphene by the electric field effect. A perpendicular magnetic field is added on graphene. Transport experiments are carried out by either sweeping the magnetic field under certain back gate voltages or sweeping $V_g$ under certain magnetic fields in a typical temperature range from 4 K to 300 K.

At zero magnetic field, gate voltage $V_g$ sweeps from positive to negative values across the transition region near the Fermi level, graphene shows an ambipolar electric field effect such that electrons or holes can be induced in concentrations up to $10^{13} cm^{-2}$ [153]. Graphene conductivity $\sigma$ increases with the increase of $V_g$ for both carrier polarities, and the Hall effect inverts its sign at around the transition region. The induced carriers (either electrons or holes) are mobile and not trapped in graphene.

The carrier mobility ($\mu = \sigma/ne$) varies from several thousand up to $15,000 cm^2/Vs$, fairly independent of temperatures between 10 K and 100 K. The mobilities are probably limited by intrinsic defects in graphene and the graphene surface morphology that is modulated by the contaminants on the $SiO_2$ layer beneath [153].

### 3.3.1 Anomalous Quantum Hall Effect in Single-layer Graphene

Magneto-oscillations can probe energy spectra in metals and semiconductors. In a typical two dimensional semiconductor system, carriers are described by the Schrödinger equation with a parabolic dispersion relation $E = \hbar^2 k^2/2m$, where $m$ is the effective mass. In a perpendicular magnetic field, the energy spectrum is quantized into discrete energy levels expressed as $E_N = \hbar w_c(N+1/2)$, with a cyclotron frequency $w_c = eB/m$. The levels labeled

$N$ are called Landau levels (LLs). The electronic states are degenerate at discrete subbands at energy levels of $E_N$. When the magnetic field rises, the energy separation between adjacent Landau levels increases, and the number of states in each subband increases. Since the total number of states is fixed, the total occupied subband number $\nu$ decreases with the rising magnetic field. As a result, the longitudinal magnetoresistance oscillates as a function of magnetic field, known as Shubnikov-de Haas oscillations (SdHos). The minimum longitudinal magnetoresistance peaks occur when the Fermi level lies between Landau levels. In strong magnetic fields, Hall conductivity shows plateaus at values of $\sigma_{xy} = ne^2/h, n = 1, 2, 3\ldots$, where $n$ corresponds to the number of occupied single spin degenerate Landau levels. These Hall plateaus accompany the minimum peaks of the longitudinal magnetoresistance. This phenomenon is called integer quantum Hall effect (QHE). The minimum longitudinal resistance of almost zero indicates that carriers can travel a long distance without losing their momentum. This ballistic transport behavior is contributed by the edge states located at the two edges of a sample. No current flows inside the sample, and these edge states carry current in opposite directions along opposite edges. Because there is no spatial overlap between forward and backward propagating edge states, carriers travel without backscattering. Thus, an almost zero resistance appears in the quantum Hall region.

In single-layer graphene, carriers are massless Dirac fermions with a linear energy dispersion relation $E = \hbar V_F |k|$. In a magnetic field, the quantization of the graphene energy spectrum is described by $E_N = \pm V_F\sqrt{2e\hbar BN}$, where $\pm$ refers to electrons and holes [57, 67]. The unusual Landau level structure with a square root dependence on B is a direct consequence of the linear density of states near the Dirac points, the most direct evidence for Dirac fermions in graphene. The Dirac-like dynamics of graphene results in a half-integer quantum Hall effect (half-integer QHE), $\sigma_{xy} = \pm 4e^2/h(N + 1/2)$, where $N$ is the Landau level index and factor 4 reflects double valley and double spin degeneracy. (In low magnetic field, each Landau level $E_N$ is four degenerate due to the a twofold spin degeneracy and twofold valley (K and K') or sublattice symmetry degeneracy.) The hallmark of half-integer QHE in graphene is the QHE plateaus at Hall conductivity $\sigma_{xy} = \pm 4e^2/h(N + 1/2)$ in

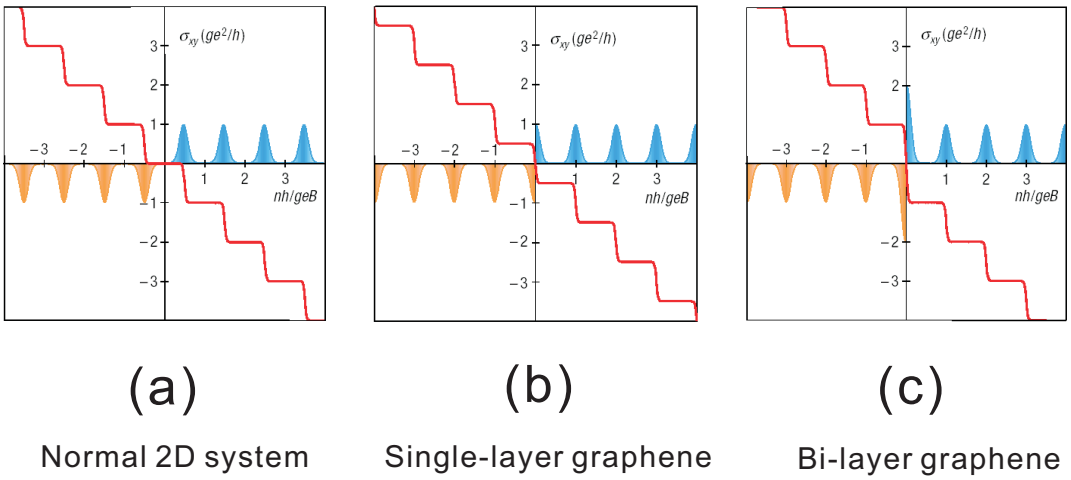


**Figure 3.3:** Schemes of three types of quantum Hall effects [156]. Red line is Hall conductivity as a function of Landau level $N$. Blue (electron) and orange (hole) regions are state densities as a function of Landau level $N$. $g$ is the degeneracy for each type of QHE. (a) Integer QHE in normal 2D semiconductor systems. (b) Half-integer QHE in single-layer graphene. (c) Anomalous integer QHE in bi-layer graphene.

Figure 3.3(b). The half-integer QHE in graphene is caused by the quantum anomaly at the $N$=0 Landau level, where it has only half of degeneracy of $N$=1 level [67, 153, 254].

This phenomenon can also be explained by the Berry's phase theory [130]. The coupling between pseudospin and orbital motion gives rise to a geometrical phase (Berry's phase) accumulated along cyclotron orbits [153, 254]. For fermions completing cyclotron orbits, Berry's phase affects the phase of SdHos. In a conventional 2D system, Berry's phase is zero. While in single-layer graphene, there is a $\pi$ phase shift of SdHos, corresponding to half-integer QHE step shift in $\sigma_{xy}$.

QHE was also observed in graphene at room temperature [155]. The Hall conductivity $\sigma_{xy}$ shows a clear plateau of $2e^2/h$ for both electrons and holes, and longitudinal conductivity $\sigma_{xx}$ approaches zero. The Fermi level resides between the lowest Landau level and the first excited level with an activation energy $\Delta E$ =600 K. The survival of QHE in room temperature can be explained by several factors: a large cyclotron gaps ($\Delta E = \hbar w_c$) characteristic to Dirac fermions in graphene, a very high carrier concentration with only a single 2D subband occupied, and high mobility at room temperature [155].

### 3.3.2 Anomalous Quantum Hall Effect in Bi-layer Graphene

Bi-layer graphene has another kind of QHE, different from the half-integer QHE in single-layer graphene. Compared to semiconductors with a conventional QHE, bi-layer graphene also has the standard Hall plateau $\sigma_{xy} = \pm N4e^2/h$ [57, 156], but the first plateau at $N$=0 is missing. The missing plateau at $N$=0 implies that bi-layer graphene is metallic at the Dirac points, which is confirmed by bi-layer graphene band structure calculations [10, 65]. The origin of the zero-level anomaly in bi-layer graphene is from the coupling between two graphene layers where A, B sublattices in these two layers are not equivalent as in single-layer graphene. The coupling causes the transition from massless Dirac fermions in single-layer graphene to massive Dirac fermions in bi-layer graphene. Carriers in bi-layer graphene obey a parabolic spectrum $E = \hbar^2k^2/2m$, where $m = 0.05m_e$, $m_e$ is the electron mass [156]. In a magnetic field, the energy quantization of bi-layer graphene energy is described by $E_N = \pm\hbar w\sqrt{N(N-1)}$ [121]. It is obvious that the zero-energy level is doubly degenerate with $N$=0 and $N$=1. Taking two valley and two spin degeneracy into account, the additional double degeneracy at zero energy not only causes the missing of the $N$=0 plateau but also the double height step ($2 \times 4e^2/h$) near the zero-energy region in Figure 3.3(c).

In bi-layer graphene, Berry phase is $2\pi$ that is indistinguishable for N$\geq$1 level, but reveals itself in the double degeneracy of $N$=0 Landau level. An external electric field on bi-layer graphene can induce a band gap between the valence band and the conduction band [120]. This makes the bi-layer graphene the only known semiconductor with a tunable energy gap.

### 3.3.3 Minimal Conductivity

Both single-layer and bi-layer graphene show a surprising minimal conductivity in order of $e^2/h$ per valley per spin near the Dirac points where the carrier concentration approaches zero [153, 156]. Theories predict a minimal conductivity of $\sigma_{min} = e^2/h\pi$ [39, 91, 165] that is about $\pi$ times smaller than what is observed in single-layer and bi-layer graphene by Geim's group [57, 153, 156]. The difference between experiments and theories maybe due

to the theoretical approximations, experimental data inaccuracy, sample inhomogeneity, and electron-hole puddles near the Dirac points [57]. The minimal conductivity is believed to link with the suppression of localization in carrier transport. For 2D Dirac fermions, localization caused by disorders is suppressed, and charge carriers cannot be confined by potential barriers that are smooth at the atomic scale.

### 3.3.4 High Field Degeneracy Splitting

In a low magnetic field, Landau level in graphene is fourfold degenerate (two spin and two valley degeneracy). The filling factor at each plateau is $v = \pm 4(N + 1/2)$. For high quality graphene samples, the fourfold degeneracy is lifted up in a high magnetic field [251]. The QH plateaus at high field were observed at filling factor $v$=0, $\pm$1, $\pm$4 in magnetic fields B>20 T at T=1.4 K. Based on their experiments, Zhang, et al., attributed the $v = 0, \pm 1$ plateaus to fully lift the spin and valley degeneracy at the lowest Landau level ($N$=0) into four subbands. And the $v = \pm 4$ plateau was explained by the lifting of the spin degeneracy at the $N$=1 Landau level [251].

To explain these new QH plateaus at $v = 0, \pm 1$ and $\pm 4$, different theoretical groups have proposed different mechanisms. Some attribute it to valley (spin) ferromagnetism, relying on the interactions between electrons [7, 50, 54, 58, 152]. Alicea, et al., argue that the ferromagnetism may not be realized in current samples that remain paramagnetic due to strong disorders that destroy exchange interaction between electrons. With the absence of interactions between electrons, the Zeeman effect becomes the only mechanism for lifting spin degeneracy. Alicea, et al., claim that the Zeeman splitting, together with symmetry-breaking interactions (valley splitting mechanism) in principle can explain the above new QH plateaus at $v = 0, \pm 1$ and $\pm 4$ in a paramagnetic system [7]. Fuchs, et al., study the electron-lattice interaction in graphene and explain that the valley degeneracy lifting may be caused by magnetic field induced out-of-plane lattice distortion [54]. Studies in this field are still in progress.

### 3.3.5 Suppression of Weak Localization

The disorder effects on transport properties of graphene have been studied by different groups [6, 93, 122, 134, 171]. Disorders originate from different sources like vacancy, dislocations, impurities, chemical dopants, and charges trapped on the surface [32].

Before discussing that, several concepts related to disorders are worthy of mention: weak localization (WL), electron-electron interference (EEI), and universal conductance fluctuations (UCF). Effects of WL, EEI, and UCF contribute to quantum corrections to the electrical conductance that is calculated from the classical Boltzmann transport theory.

Weak localization (WL) is a low temperature phenomenon. It originates from the interference effects between elastically time-reversed scattered carrier waves, which results in a backscattering probability enhancement [20]. There are two main features of the WL effect: a negative magnetoresistance in low fields and a logarithmic temperature dependence of resistance at low temperatures. The WL effect is more pronounced for 2D system than for 3D systems and also has been observed in thin metal films, heterostructures, graphite, and GICs [15, 131, 198]. From the WL measurement, some characteristic parameters of samples can be derived, such as phase relaxation time (or inelastic scattering time) and elastic scattering time [223]. Inelastic scattering processes such as electron-phonon interactions at fairly high temperatures will destroy the phase coherence between elastically scattered carrier waves and suppress the WL. A small external magnetic field can also break the phase coherence between carrier waves. So the WL phenomenon disappears with a small perpendicular magnetic field and/or a rise in temperature.

The electron-electron interference (EEI) effect is due to mutual Coulomb interactions of electrons. EEI also leads to a similar logarithmic temperature dependence of resistance as WL. But the EEI effect is not strongly suppressed by a small perpendicular magnetic field, which distinguishes EEI from WL.

Universal conductance fluctuations (UCF) are due to phase coherent interference by scatters in samples. UCF shows a specific oscillation pattern as a fingerprint for an individual sample because the scatter distribution in one sample is different from that in another. UCF occurs when the phase coherence length $l_\varphi$ is larger than or comparable to the mean

free path $l_e$. The most remarkable feature of UCF is that the amplitude of conductance oscillations is within a universal scale of $\delta G = e^2/h$ regardless of sample size. In contrast to WL, UCF is not rapidly smeared away at a small magnetic field.

To study the electronic and transport properties, the concept of scatters is used to describe the local potential barriers that exist in a system. Scatters can be categorized into short-range and long-range scatters. In the case of short-range scatters, the range of scattering potential is smaller than the lattice constant. In the case of long-range scatters, the range of scattering potential is larger than or comparable to the lattice constant but much smaller than the typical electron wavelength [255]. The influence of these two kinds of scatters on the density of states, state localization [171] and the conductivity in graphene has been studied extensively in the absence or presence of a magnetic field [32, 59, 164, 194, 210, 255].

Graphene with Dirac particles naturally preserves the property of weak anti-localization. Dirac particles have the chiral nature which originates from the equivalence of A, B sublattices on a graphene sheet. The term of pseudospin is assigned to describe this chirality. Like spin, pseudospin has two values. Different from spins, the pseudospin is coupled to momentum by a relation of $\frac{\sigma \cdot p}{|p|} = \pm 1$ (in the case of electron carrier, '+' for K valley and '-' for K' valley. ). In order to reverse the direction of momentum by scattering, the pseudospin has to be reversed at the same time. However, intravalley scattering (or long-range scattering) between A and B can't reverse the value of pseudospin because of the equivalence of A,B sublattices. Thus direct backscattering is not inherently favorable in a clean graphene unless intervalley scattering happens by the involvement of more short-range defects.

## *3.4 Graphene Devices and Possible Applications*

When I started to study epitaxial graphene in 2003, graphene has not been observed in experiment. The immense interest in graphene from our group was triggered by the urgent demand of finding new quantum era materials. We think that epitaxial graphene can be chosen as one of next generation semiconductor materials.

As we know, the standard Si technology is reaching its feature size limitation of tens of

nm where classic transport theories and standard semiconductor materials fail to function properly due to quantum size effects. Several material candidates have been proposed to overcome these limitations in Si technology. Among them, carbon nanotubes (CNTs) attract a lot of attention because their excellent electronic, thermal, optical, and mechanical properties. However, several key problems hinder CNT from real applications. First, the typical growth methods of carbon nanotubes can not find ways to precisely control carbon nanotube type (metallic or semiconducting), direction, and helicity, etc. Defects can be induced during the preparation process or the following purification process [63]. Second, CNTs are proposed as interconnections and channel material in FETs [12, 182]. However, CNTs have to be connected with each other individually, and contact resistance is unavoidable. Consequently the coherent and ballistic transport properties of CNTs can't be fully realized.

In fact, most of the electronic properties of CNTs are comparable to those in graphene narrow ribbons. A graphene ribbon can be pictured as an unrolled carbon sheet. More than that, graphene has its peculiar properties that are mainly owing to its massless Dirac spectrum and edges states along the graphene ribbons' boundaries. The type and orientation of graphene ribbons can be in principle controlled by local lithography patterning. As a 2D platform, graphene can be fairly easy to integrate with standard IC fabrication processes.

In the past several years, exfoliated graphene has been investigated for possible device applications. Below, I will review the research on exfoliated graphene, including field effect transistors (FETs), spintronics, superconductivity, and ballistic transport, etc.

### 3.4.1 Graphene Nanoribbons (GNRs)

Graphene nanoribbons (GNRs) have three kinds of terminating edges: zigzag, armchair, and chiral [139, 228, 229]. The edges of GNRs could be free or bonded by different functional atoms or molecules, and mostly determine the electronic, optical, magnetic, and transport properties of GNRS [179, 213, 229]. The method of tight-binding approximation [11, 25, 106, 158], density function theory [13], and *ab initio* [213] have been applied to calculate properties of GNRs regarding to edge shape, ribbon width, disorder, magnetic field, and

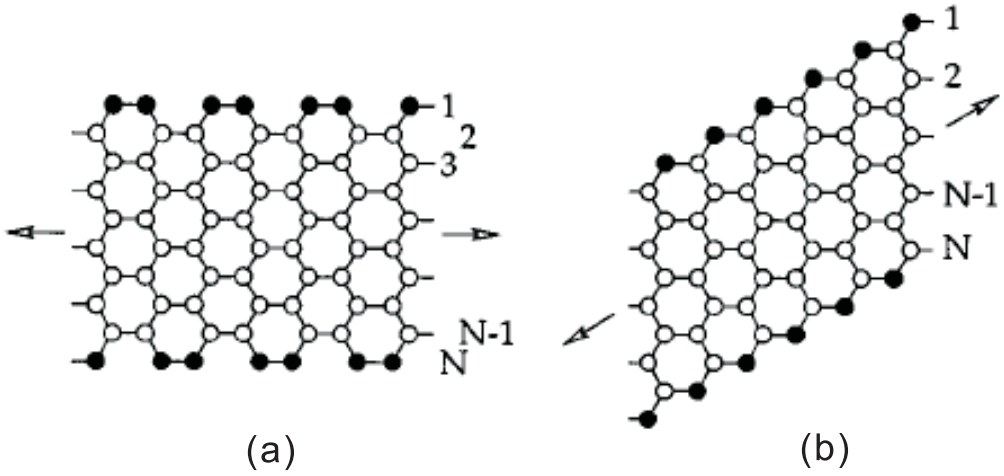


**Figure 3.4:** The edge types of graphene nanoribbons. N is the ribbon width. (a) Armchair. (b) Zigzag. [139]

electric field.

The metallic or semiconducting properties of GNRs are determined by edge type ( zigzag or armchair) and ribbon width (N). Two types of idealized edges have been usually considered: armchair and zigzag. Figure 3.4 shows the structures of GNRs with zigzag edges and armchair edges. From tight-binding calculations, the zigzag ribbon is metallic for any ribbon width. The most remarkable feature of zigzag ribbons is the presence of a partly flat bands at the Fermi level where the states are localized near the edges, so called edge states. The edge state has a nonvanishing amplitude only on one of the two sublattices, and have nonbonding character. However, in a narrow ribbon with zigzag edges on both sides, the edge states localized on both sides have finite overlap that results in bonding and antibonding states by hydrization of $\pi$ electrons [230]. The slight dispersion caused by edge state overlap provides one conducting channel for electron transport except at exactly $E = 0$. That make zigzag ribbons metallic. An armchair ribbon is metallic or semiconducting depending on its ribbon width of N [230, 139]. An armchair ribbon is metallic when N=3m-1, where m is an integer. Otherwise, an armchair ribbon system is semiconducting and the magnitude of the gap is inversely proportional to the ribbon width N. No localized edge states appear on the armchair GNRs.

Researchers have explored the possible properties owned by GNRs, including ballistic

transport, bandgap, coherent and quantum transport, magnetism, etc.

Areshkin, et al., studied the ballistic transport in metallic armchair- and zigzag-edge graphene nanoribbons [11]. Both types of ribbons have outstanding ballistic transport properties in the presence of substrate-induced disorder. The zigzag-edge ribbons can retain these properties even with irregular shape edges, which indicate zigzag GNRs to be a better candidate for ballistic device applications.

Barone, et al., presented a systematic density functional theory study of semiconducting armchair GNRs [13]. Armchair GNRs with a width of 1-3 nm are predicted to have band gaps similar to those of Ge, InN, Si, inP, or GaAs [13]. GNRs with widths larger than 8 nm present a maximum bandgap of 0.3 eV. While for ribbons with a width of 80 nm, the maximum possible band gap is 0.05 eV. The band gap oscillates as a function of the widths of armchair GNRs [47]. Son, et al., compared the band gaps induced in both hydrogen-passivated zigzag and armchair GNRs as a function of ribbon width [202]. Their calculations reveal that both types of ribbons show band gaps but from different origins. The energy gaps for CNRs with armchair edges arise from the both crucial effect of the edges and quantum confinement. For GNRs with zigzag edges, energy gaps are caused by the staggered sublattice potential on the hexagonal lattice. The energy gaps of zigzag and armchair graphene nanoribbobs decreases as ribbon widths increase.

Coherent and quantum transport in graphene nanoribbons also attracts a lot of attention in literature [135, 171, 231, 228]. Peres, et al., found that for a ultra clean graphene at low biases in low temperatures, armchair and zigzag systems showed conductance quantization [171]. Munoz-Rojas, et al., studied the effect of structural nanoconstriction on the coherent transport properties of ideal zigzag long graphene nanoribbons, as a resemblance to study quantum point contact in an all -carbon single-molecule junction [135]

The edge states also play important roles in magnetic properties of GNRs [229]. Ferromagnetism on graphene zigzag ribbon has been studied. It is calculated out that edge states localized near the zigzag edges causes a ferromagnetic spin polarization localized at the edge sites even in the very weak Coulomb interaction [230].

### 3.4.2 2D Graphene Field Effect Transistor and Band gap: Experimental Review

A graphene sheet doesn't have an energy gap since it is a zero-gap semiconductor. The back gating on exfoliated graphene multilayers (Bernal stacked) shows its ambipolar properties with the coexistence of electrons and holes near the Fermi level [154, 253]. The back gating on single-layer and bi-layer graphene also reveals a minimal conductivity ($e^2/h$) at the Dirac points where the charge carriers almost diminish to zero [153, 156].

Different groups have tried different approaches to observe energy gaps on GNRs. Prof. Philip Kim's group in Columbia University reported the relations between the energy gap and the ribbon width ranging from 14 to 63 nm. They found that energy gap was inversely proportional to the ribbon width without a clear signature of crystallographic direction dependence. The derived fitting relation is $E_{gap} = \alpha/(W - W^*)$, where $\alpha = 0.02$ eV $\cdot nmand$W$^* = 16$ nm [70]. The energy gap can be as large as 200 meV on a ribbon of about 15 nm wide. Since the device fabrication process can not control the edge shape of ribbons, the theoretical prediction for GNRS is not observed. Chen, et al., in IBM Research fabricated graphene nano-ribbon FETs in a width range of 20-100 nm, and investigated the electrical properties as a function of ribbon width, temperature, and the back gate voltage. They found that the impact from ribbon boundaries was non-negligible at room temperature when the ribbon width was narrower than 50 nm. The mechanism of boundary effect may attribute to more scatterings on the rough boundaries of a narrower ribbon [35]. A gap of 28 meV was extracted out for a 20 nm wide ribbon due to energy quantization induced by the geometrical confinement. The bandgap is rather small and it is easily to be smeared away by thermal carriers at high temperature.

The above energy gaps measured in GNRs may be explained in terms of Coulomb blockade. Electron interactions play a decisive role at the quantum dots which are formed by the presence of necks due to the rough ribbon edges [201]. Recently, Prof. Hongjie Dai's group reported a chemical route to produce GNRs with width below 10 nm. The on/off ratio of FETs fabricated on their sub 10 nm GNRs was about $10^7$ at room temperature. The hole mobility in FETs was estimated to be $\sim 100 - 200 cm^2/Vs$ [110].

Lemme, et al., reported a top gated FET device manufactured on a wide graphene ribbon (265 nm) [107]. Compared with uncovered graphene with a mobility $\mu \sim 5000 cm^2/Vs$, the graphene coated with a 300 nm $SiO_2$ dielectric layer had a lower mobility of $\sim 500 - 700 cm^2/Vs$) due to the interaction between graphene and the $SiO_2$ layer. But the mobilities of $SiO_2$ coated graphene were still larger than silicon transistors, more significant when compared to ultra thin silicon film on insulators [107].

Graphene p-n, n-p-n, or n-p-n-p junctions have been realized on exfoliated graphene FETs by applying a global back side gate and local top gates [84, 169, 235]. New quantum Hall effect in gate-controlled p-n or p-n-p graphene junctions have been observed and discussed [1, 169, 235].

A Gate-tunable bandgap was also observed in bi-layer graphene devices. Bilayer graphene itself is zero gap. In order to open a gap, the inversion symmetry in the graphene plane must be broken by making the onsite energies of the A and B atoms different. This inversion symmetry breaking can in principle be implemented by an external electric field. From the work of Oostinga, et al., a possible gap of below 10 meV was measured their bi-layer graphene devices [163].

### 3.4.3 Graphene Spintronics

Spintronics is a multidisciplinary field whose central goal is to actively manipulate the spin degree of freedom in solid-state systems. Spin transport is different from charge transport in that spin is a nonconserved quantity in solids due to the spin-orbit interaction and the hyperfine coupling. For an operational spin device, three fundamental issues in semiconductors are required to solve. First, spin scattering length should be larger than the device size so that the spin orientation is not destroyed. Second, spins can be injected into the current channel then be detected between the electrodes. Third, efficient ways are needed to control the spin population and orientations externally, for example by a gate.

Spin in single- and few-layer graphen shows peculiar properties in magnetism [81, 97, 152] and transport [151, 199, 217]. That is mainly caused by the massless Dirac spectrum of graphene and edges states localized along the boundaries of graphene ribbons. Magnetism

with localized spin momentums is expected in zigzag GNRs with edge states [55, 97, 118]. According to different calculations, ferromagnetic spin structure exists at the hydrogenerated zigzag edges [55, 97]. Ferromagnetic instability in graphene was also studied [172].

In spin transport theory, graphene exhibits spin Hall effect without breaking the time-reversal symmetry (TRS) [192, 199]. The spin-orbit interaction opens a gap near the Dirac points. Such a gap breaks TRS individually for each spin species, but leaves the whole systems invariant [192]. At sufficiently low energies near the Dirac points, graphene is predicted to exhibit a spin quantum Hall effect (SQHE) with an energy gap generated by the spin-orbit interaction [89, 193]. In theory, spin qubits in graphene quantum dots have been proposed for quantum computation and distant communication because of the fairly long spin coherence time and fast operating time of spin qubits [219].

In spin transport experiment, spin valve effect in graphene has been demonstrated [82, 151, 217]. In the experiment of Hill, et al., soft magnetic NiFe electrodes were used to inject polarized spins into graphene, and a 10 % change in resistance was observed as the electrodes switched from the parallel to the antiparallel state [82]. Owing to the negligible spin-orbit interaction, spin polarization in graphene can survives over submicron distance. In the experiment of Tombros et al., the spin transport was relatively insensitive to temperature. Non-local measurement showed that spin coherence length extended beneath the ferromagnetic electrodes. The spin relaxation length was about 1.5-2 $\mu m$ at room temperature [217].

### 3.4.4 Superconductivity

Graphene is not a natural superconductor. But proximity effect could be induced in graphene when graphene is contacted with superconducting electrodes [16, 23, 78, 216]

In theory, owing to the Josephson effect, a supercurrent can flow through a normal metal region between two closely spaced superconducting electrodes. Titov and Beenakker predicted that a supercurrent (dissipationless current) can sustain in a superconductor-metal-superconductor (SNS) junction with an undoped graphene ribbon as the metal region [216]. For supercurrent to happen, the transport in graphene should be coherent and the

time reversal symmetry must be present. The graphene Josephson junctions with zigzag and armchair edges were also studied to investigate their property dependence on edge types [132].

In experiment, bipolar supercurrent in graphene has been observed in the graphene SNS junction system with a graphene ribbon of hundreds of nm long [77].

### 3.4.5 Suspended Graphene

Free standing or suspended graphene sheets have been fabricated to minimize the influence on graphene transport from the substrates. The topography of suspended graphene sheets was checked with STM and TEM [128, 129]. The transport, optical, mechanical properties of these sheets were measured by different groups [26, 62].

From the Mermin-Wagner theorem, no long-range order exist in two dimensions at finite temperatures. TEM images on suspended graphene sheet showed that the graphene sheet itself was not perfectly flat in the plane with about 1 nm out-of-plane wiggles [128].

Single-layer and multi-layer graphene resonators were fabricated and measured in the MHz range with the electrical or optical modulation in high vacuum to reduce the damping effect of the air. A single-layer graphene gave a qualify factor of 78, indicating a possible limit range for two-dimensional nanoelectromechanical systems [26].

### 3.4.6 Key Issues for Graphene Applications

Before graphene marches into the industrial world, several issues have to be carefully clarified or solved in labs. They include

- Cheap, reliable, and repeatable methods to fabricate graphene,
- Fast and accurate techniques to identify and characterize graphene,
- Edge type selection and doping control on graphene ribbons, and
- Integration with Si technology

For the first issue, epitaxial graphene grown on substrates is the most promising choice. The method of mechanical cleavage of bulk graphite has the problems of small size, random distribution, and substrate sensitivity [154]. Although exfoliated graphene works well for physical study and device demonstration, it is far beyond the consideration of industrial engineers. Epitaxial growth methods have been widely utilized in the semiconductor material preparation such GaAs and InP. From the literature, amorphous carbon films or nanosize graphite flakes can be grown on substrates by physical deposition methods (such as pulsed laser ablation from a bulk graphite target [29]), or chemical methods including decomposition of hydrocarbon gas [29, 137, 233], disproportionation of CO gas with the aid of iron catalyst [136]. Recently High quality graphite films have been grown on Ru, Ni, or Pt metal films by chemical reaction of hydrocarbons [159, 160, 250]. But these conducting metal films are hard to remove in order to make use of graphite layers on top of them. Multilayer graphene films can epitaxially grow on SiC substrates by thermal decomposition of SiC at high temperature in ultra high vacuum (UHV). This method was initially reported by surface scientists. In fact, multilayer graphene films can grow in a our homemade, low-pressure, vacuum furnace. The lattice match between 4H-, 6H-SiC and graphene demonstrates SiC as a very good substrate to grow high quality graphene sheets, which have been confirmed with surface analysis tools (AFM, SEM, LEED, Auger, and X-ray) and transport measurements.

For the second issue, in the short run, Raman spectroscopy is so far the most promising technique to identify the layer number of FLG. The method of the phase contrast optical microscopy can be utilized for a rapid scan on a substrate to identify graphene flakes. In the long run, with the improvement on epitaxial growth of graphene, the thickness of FLG can be precisely modulated by the experimental factors such as gas species, pressures, temperatures, and substrates.

For the third issue, STM images on graphene ribbon show random zigzag, armchair sequence edge boundaries [95, 146, 147]. To control the edge type, chemical selective etching on ribbon boundaries may favor one kind of edge type than the other one. Chemical doping can also modify the edge states.

For the last issue, it will not become a problem if epitaxial graphene can grow on Si, $SiO_2$ or other semiconductor substrates. To implant epitaxial graphene grown on SiC to a Si wafer, one possible way is by the 'smart-cut' technology that requires a ultra clean and flat surfaces on both SiC and Si wafer, a fine-tuned ion implantation, and careful operations.

## *3.5 Summary*

Graphene is a zero bandgap semiconductor with Dirac-particle carriers. It owns many peculiar properties such as anomalous quantum Hall effect on single- and bi-layer graphene, minimal conductivity, degeneracy splitting in high magnetic field, and weak anti-localization. Carriers in graphene has a high mobility of $\sim 10^4 cm^2/Vs$, even down to several nm size. The ongoing research topics on graphene devices and possible applications are briefly reviewed to exhibit all the possibilities of graphene. With my best understanding, key issues for the real applications of graphene are discussed at the end.

# CHAPTER IV

# SILICON CARBIDE

Silicon carbide (SiC) is an indirect wide band gap semiconductor. SiC receives substantial interest from scientists and engineers because of its unique physical and electronic properties. Here, 4H- and 6H-SiC are chosen as the substrates for the epitaxial graphene growth. This chapter will introduce the crystal structures, polytypes, physical, and electronic properties of SiC. The bulk growth of SiC boules and epitaxial growth of SiC epilayer are described to provide a better understanding of epitaxial graphene growth on SiC.

## *4.1 Crystal Structure and Polytype of Silicon Carbide*

SiC crystal is composed of the same number of Si atoms and C atoms. The element unit of SiC crystal structure is a covalently bonded tetrahedron with 4-fold symmetry. Through $sp^3$ hybridization, each Si atom is surrounded by four C atoms and vice versa. In Figure 4.1(a), the distances between Si-C bonds and Si-Si bonds are 1.89 Å and 3.08 Å, respectively. With the definition of C-axis along one of Si-C bonds, the crystal can be pictured as being composed of Si-C bilayers along the C-axis. A single Si-C bilayer has a planar sheet of Si atoms coupled with a planar sheet of C atoms. The distance between two adjacent Si-C bilayers is about 2.5 Å. Cutting the SiC crystal perpendicular to the C-axis results in two different polar faces: (0001), Si atom terminated face (Si-face), and $(000\bar{1})$, C atom terminated face (C-face) (See Figure 4.1(b)).

SiC has more than 170 polytypes. Different polytypes of SiC consist of different stacking sequences of Si-C bilayers along the C-axis. Along the stacking direction, adjacent bilayers shift with respect to each other. If each Si-C atom pair is represented as a sphere, each layer of spheres along the C-axis can occupy three different positions labeled A, B, and C in Figure 4.1(c). One can assume the spheres in the first layer are at position A. In the closed packed structure condition, the next sphere layer can be placed on the top of layer A at position B (or C). The third one can be placed at position either C or A (or either B or A).

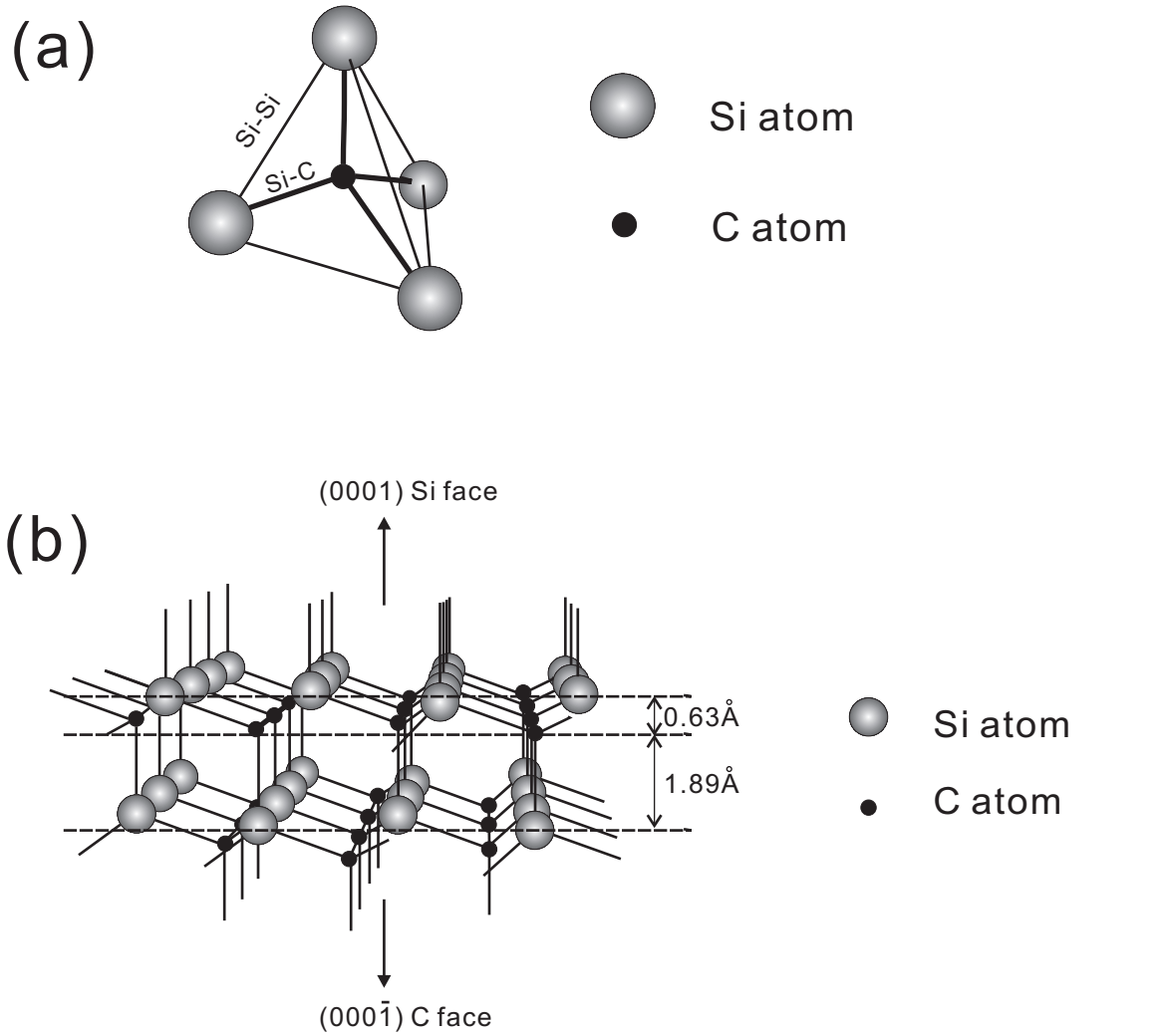


**Figure 4.1:** (a) The tetrahedral structure of the Si and C atoms in SiC. (b) Crystal structure with Si-C bilayers along the C-axis [0001] direction. The plane is (11$\bar{2}$0). (c) Possible stacking positions in a closed packed hexagonal SiC structure.

The stacking sequence of a unit cell repeats to construct into a whole crystal of a certain polytype. There are two stacking kinds of Si-C bilayers: (111) cubic structure (zincblende) and (0001) hexagonal structure [104].

Two notation methods have been used to describe SiC polytypes. The first method was proposed by Jagodzinski [86], in which each bilayer is described in either a local cubic (k) structure or hexagonal (h) structure. The nearest neighbors of a Si (or C) are tetrahedrally arranged, but the next nearest neighbors may be designated in a hexagonal or cubic structure. If the centroids (the center atoms of tetrahedrons) are at the same positions for two bilayers above and below, this structure is hexagonal. For example, a stacking sequence AB is purely hexagonal and is labeled as h2. If the positions of the centroids in two bilayers above and below are different, this structure is cubic (k). For example, a stacking sequence ABCABC is purely cubic and is labeled as k3.

The second and most used notation method was proposed by Ramsdell and is based on the hexagonal symmetry [180]. In this number-letter notation, the number describes the number of layers in a complete unit cell along the C-axis, and the letter describes the Bravais lattice type (hexagonal (H), cubic(C), or rhombohedral (R)). There are five basic polytypes with small stacking periods: 2H, 3C, 4H, 6H, and 15R [104]. Figure 4.2 shows the stacking sequence of the 2H, 3C, 4H, and 6H unit cell structures. Other polytypes with longer periods can be considered as a combination of these five basic stacking periods.

2H-SiC has the pure hexagonal structure (Wurtzite) with the AB stacking sequence, and 3C-SiC has the cubic structure (zincblende) with the ABC stacking sequence. 3C-SiC is also referred as $\beta$-SiC. And non-cubic polytypes of SiC are sometimes ambiguously referred as $\alpha$-SiC. For a cubic crystal structure, three Miller indices, hkl, are used to described the lattice direction and planes in the crystal. They are integers with the same ratio as the reciprocals of the intercepts with x, y, z axes, respectively. Four principle axes of $a_1$, $a_2$, $a_3$, and $c$ are used to describe a hexagonal crystal structure. Here $a_1$, $a_2$ and $a_3$ are in the same plane with 120 degrees angles between each other: $a_1+a_2=-a_3$, and C-axis is perpendicular to this plane.

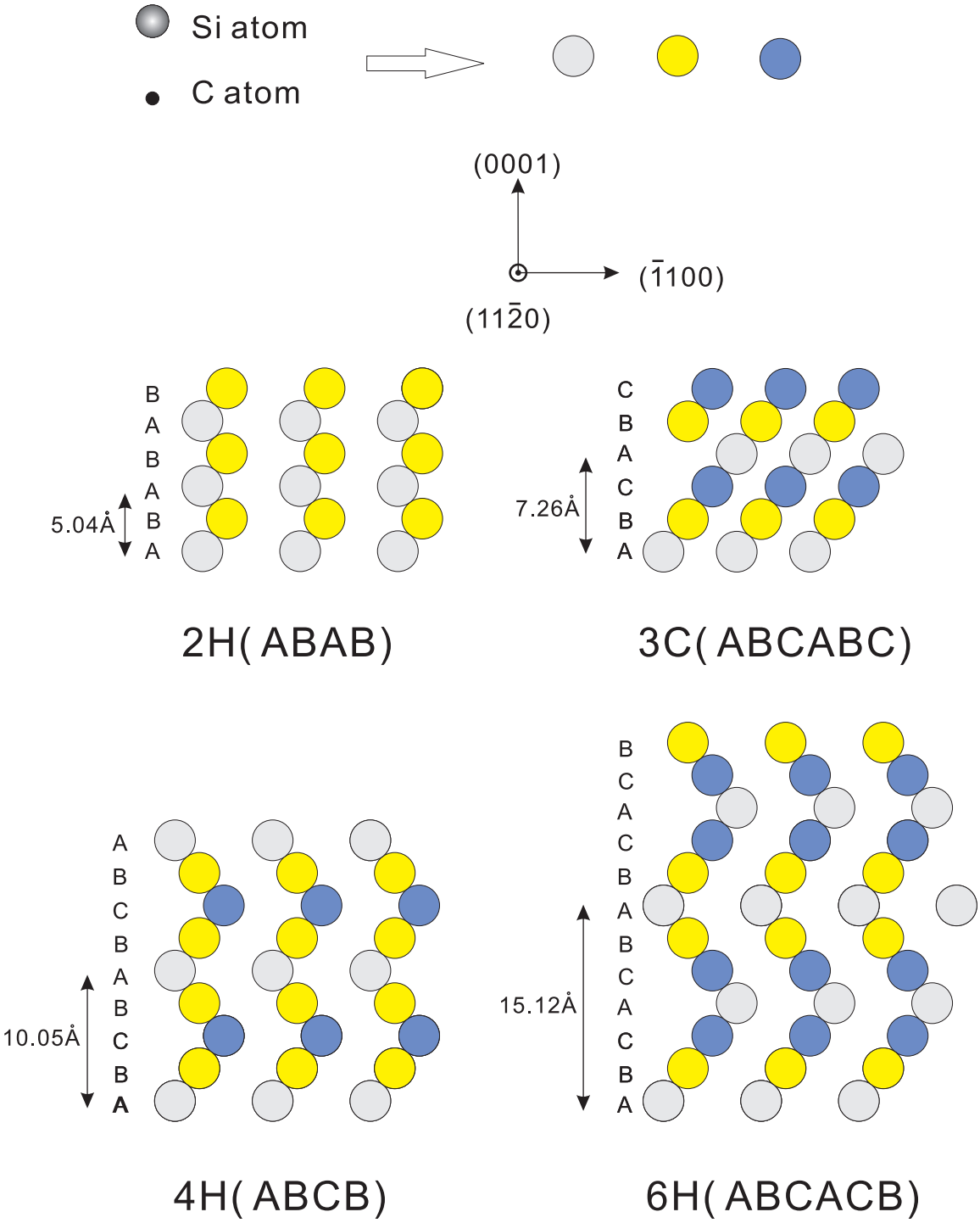


**Figure 4.2:** Stacking sequences of the 2H(AB), 3C(ABC), 4H(ABCB) and 6H(ABCACB) SiC polytype in the (11$\bar{2}$0) plane.

**Table 4.1:** Properties of SiC polytypes in comparison with Si and GaAs at room temperature. [27, 46, 143, 248]

| Property | Si | GaAs | 4H-SiC | 6H-SiC | 3C-SiC |
|---|---|---|---|---|---|
| Bandgap $E_g$(eV) | 1.1 | 1.42 | 3.2 | 3.0 | 2.3 |
| Intrinsic carrier density $n_i$ $(cm^{-3})$ | $10^{10}$ | $1.8 \times 10^6$ | $10^{-7}$ | $10^{-5}$ | 10 |
| Relative dielectric constant $\epsilon_r$ | 11.9 | 13.1 | 9.7 | 9.7 | 9.7 |
| Electron mobility $\mu_n$ $(cm^2V^{-1}s^{-1})$ | 1200 | 6500 | ∥ c-axis: 800, ⊥c-axis: 800 | ∥ c-axis: 60, ⊥c-axis: 400 | 750 |
| Hole Mobility $\mu_h$ $(cm^2V^{-1}s^{-1})$ | 420 | 320 | 115 | 90 | 40 |
| Breakdown electric field $E_c$(MV/cm) | 0.6 | 0.6 | ∥ c-axis: 3.0 | ∥ c-axis: 3.2 | 2.2 |
| Saturated electron velocity $V_{sat}$ $(10^7 cm/s)$ | 1.0 | 1.2 | 2 | 2 | 2.5 |
| Thermal conductivity $(Wcm^{-1}K^{-1})$ | 1.5 | 0.46 | 3.7 | 4.9 | 4.9 |
| Lattice constant (Å) | 5.43 | 5.65 | 3.07 | 3.08 | 4.36 |

## *4.2 Physical and Electronic Property of Silicon Carbide*

The stacking sequence has a profound effect on the properties of different SiC polytypes. Among them, 3C-SiC, 4H-SiC, and 6H-SiC have been extensively studied for their favorable physical and electronic properties as shown in Table 4.1, compared with the most important semiconductors: Si and GaAs. These properties include wide band gap, high thermal conductivity, high breakdown field strength, high saturated drift velocity, etc. Thus SiC is very attractive for high-power, high-frequency, and high-temperature device applications [33, 38, 46].

As seen in Table 4.1, different SiC polytypes show significant differences in electronic properties such as the bandgap, breakdown voltage, mobility, etc. Moreover, some properties in 4H- and 6H-SiC polytypes show anisotropy in the directions along or perpendicular to the C-axis. In contrast, 3C-SiC is isotropic.

## *4.3 Growth of Silicon Carbide*

A high quality bulk SiC crystal is the first crucial step for SiC's technological application. Natural SiC is extremely scarce and found in tiny quantities in only certain types of meteorite. SiC growth has a fairly long history. In 1893 Archeson introduced an electric smelting furnace to manufacture small SiC crystals. The quality of SiC crystals was improved greatly in 1955 after Lely presented the sublimation process of producing free standing SiC platelets. The modified Lely method was reported by Tairov and Tsvekove in 1978. This growth method (also known as physical vapor transport (PVT) growth) uses a seeded crystal on which the source vapor is deposited to grow a boule of this material [214]. In 1987 Cree Research Inc. was founded and became the first commercial vendor of high quality SiC wafers as large as 4 inches in diameter. Besides the bulk SiC crystal, epitaxial SiC layers are grown on the surface of a SiC wafer to provide good structural quality and excellent doping control. Our group developed SiC as the substrate for epitaxial graphene growth.

### 4.3.1 Bulk Growth of Silicon Carbide

SiC can not be grown from conventional seeded melt-grown techniques being employed in the Si wafer production because SiC sublimes before being melted at reasonably attainable pressures and temperatures [244]. Seed sublimation growth, also known as physical vapor transport (PVT), has been the most successful method so far for growing large SiC boules.

SiC bulk crystal growth via sublimation is a complex process in which a number of parameters are involved. The crystal growth is driven by the shift along a temperature gradient between the solid SiC and its vapor. The vapor is produced via the decomposition of the SiC source material and reactions with the environment. A single crystal SiC is formed from deposition of the supersaturated vapor species on a SiC seed crystal by mass transport.

The typical growth furnace is a vertical air or water cooled quartz tube reactor with inductively heated graphite crucible [244]. A graphite foam cylinder outside the hot graphite crucible is used as a thermal shield. The crucible initially is evacuated to a pressure of $10^{-8}$

mbar with a turbo molecular pump [191]. For the SiC growth, the crucible is filled with an inert gas (such as Argon) or dopant gas (such as $N_2$) at a low pressure through a gas supply needle valve. The system can be operated in a static or gas-flowing condition.

A high-quality Lely platelets or a modified Lely grown wafer with a certain crystal orientation is employed as the seed crystal with different sizes. It is very important to obtain a high quality seed with few defects.

The crystal growth is driven by the temperature gradient between the source and the seed. The temperature gradient range from the source (at a higher temperature) to the seed (at a lower temperature) is about 20 K-30 K/cm [191]. When the SiC powder source is heated to high temperatures , it decomposes into four main gaseous species: Si, $Si_2C$, $SiC_2$, and $Si_2$ [56]. The gaseous Si has the highest partial pressure. These gaseous species are then transported to the growing surface. There are interactions between these gaseous species with the gas environment and graphite walls. A typical growth rate for bulk SiC is from 0.5 to 5 mm/hr. The growth rate is determinated by the rate of diffusive transport of the growing species from the source to the seed. The diffusion constants of the gaseous species are inversely proportional to the pressure in the crucible.

However, a variety of stacking sequences and large numbers of structural defects such as micropipes and dislocations exist in SiC crystals and epitaxial layers [245]. As shown later, these defects affect the surface morphology of SiC after hydrogen etching treatment or graphitization treatment.

1) Si droplet.

In a closed vacuum crucible, the total vapor pressure at the equilibrium is determinated by the highest partial pressure of one of the gaseous components. In the case of SiC sublimation growth, excess Si loss might occur on both the SiC source and the growing SiC seed. That causes the graphitization of the source and the seed with time, and deteriorates the SiC growth conditions. Two ways have been reported to adjust the Si vapor behavior. One way is to introduce excess Si to the SiC source to compensate for the excess loss of Si [28]. The other way is to increase the partial pressure of C vapor by a carbon getter to balance the Si/C ratio in the vapors [149].

2) Polytype occurance.

The occurance of polytype inclusion in the bulk growth is common if no special precautions are taken. Several growth parameters directly influence the growth of crystal polytypes, for example, growth temperature, temperature gradient, impurities, surface orientation, polarity of the seed, distance between the source and the seed, gas flow rate, C/Si ratio in the gas phase, and gas pressure. Some of these parameters are linked to each other and make it extremely difficult to understand and control the growth of a particular SiC polytype. In commercial production, 6H-SiC and 4H-SiC wafers appear to be free of undesired polytype inclusions. A reproducible method for 3C-SiC production is still under development.

3) Defects.

Several kinds of defects exist in grown SiC boules such as micropipes, mosaicity, dislocations, cracks, and basal plane tubes. Micropipes are unique in the SiC growth. They are described as physical holes of diameters varying from a few nm to several $\mu m$, and they can penetrate deep into the crystal. In general, micropipes are caused by internal stress originating from different reasons: screw dislocations, Si droplets or dust particles on the growing front of the seed, polytype disturbance, or a large temperature gradient [191]. If micropipes interact with the active region of a device, the performance of this device will be heavily impaired.

### 4.3.2 Epitaxial Growth of Silicon Carbide

Sublimation-grown SiC wafers are not used directly as the substrates for SiC device applications. A high quality epitaxial SiC layer over SiC or other substrates (such as Si [24, 174]) is a key issue in SiC technology. In the past two decades, several SiC epitaxial growth methods have been investigated: Chemical Vapor Deposition (CVD) [94, 119, 145], Sublimation Epitaxy (SE) [92, 212], Liquid Phase Epitaxy (LPE), and Molecular Beam Epitaxy (MBE).

Current CVD growth is the predominant method for the mass-production of epitaxial SiC wafers with respect to film thickness, uniformity, reproducibility, throughput, doping control, and high quality. In a typical CVD process, precursor gases (often diluted in carrier

gases) are delivered into a reaction chamber at an approximately ambient temperature. As precursor gases pass over, or come into contact with a heated substrate, they react or decompose to form a solid phase. The solid phases deposit onto the substrate. Gaseous by-products are transported away from the surface of the substrate and are pumped out of the chamber. CVD offers good control over the composition of the film as well as the doping profile.

Several CVD systems exist for SiC epitaxial growth with a variety of options such as hot-wall or cold-wall, horizontal or vertical orientation, atmospheric or low pressure, resistive or radio-frequency (RF) heating, etc. Here hot-wall or cold-wall refers to the temperature of the sidewall adjacent to the space of the flowing reacting gases. A typical CVD reactor is a horizontal, hot-wall, atmospheric pressure, RF heated, graphite susceptor. In a silane-propane-hydrogen gas system, the Si precursor, silane ($SiH_4$), and the C precursor, propane ($C_3H_8$), flow into the reactor with a carrier gas ($H_2$) under atmospheric pressure. To protect the graphite wall from reacting with hydrogen, a SiC layer is coated on the inner wall of the graphite susceptor. The growth temperature ranges from 1300°C to 1800°C. The growth rate of epilayer SiC is about several to tens of $\mu m$ per hour [144, 174, 176]. Epitaxial grown SiC films can be in-situ doped by nitrogen (usually $N_2$) for n-type and by aluminum (usually trimethylaluminum (TMA)) for p-type.

Homoepitaxial and heteroepitaxial growth of SiC epilayer are being investigated. Homoepitaxy means the polytype replication from the substrate to the epilayer. Homoepitaxial growth of 4H-SiC and 6H-SiC has been accomplished by step-controlled epitaxy [94]. Step-controlled epitaxy means the polytype of an epilayer can be controlled by surface steps existing on the off-axis (or off-oriented, mis-oriented) substrates, i.e. surface steps on the substrate serve as a template for replication of the same polytype in the epilayer as in the substrate. Surface morphology and polytype of the grown SiC epilayer on a SiC substrate depend on the tilt angle of the substrate, initial surface condition, growth rate, and temperature [94, 119, 177].

Powell and Neudeck [144, 176] grew step-free SiC films on device-size (0001) SiC mesas that were slightly tilted as seen in Figure 4.3. Mesas on the substrates were fabricated by

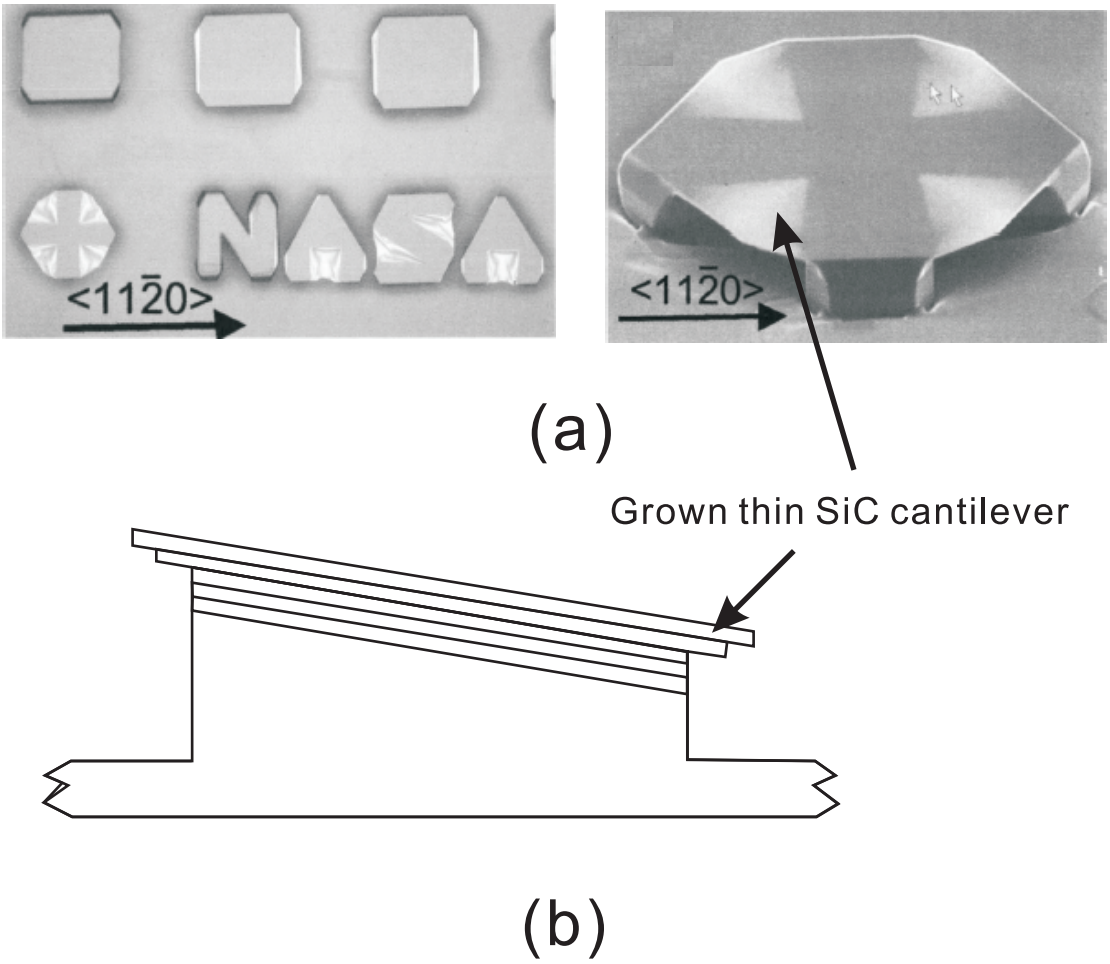


**Figure 4.3:** Step-free SiC film homoepitaxially grown on SiC mesas. (a) Optical images of grown epitaxial SiC layers on SiC mesas. (b) Schematic cross-section depiction of the SiC cantilever formation [144].

inductively coupled plasma (ICP) etching. Hydrogen etch was carried out before epitaxial growth. Thin SiC cantilevers were observed between inside corners of postgrowth mesas [144]. Postgrowth mesa shape was affected significantly by pre-growth mesa shape and orientation. Step-free surfaces were not generally observed on all mesas. If mesas initially contain screw dislocation defects, they cannot be flattened by the following epitaxial growth. Some regions on these mesas grew vertically due to the continual spiral growth of new steps emanating from where screw dislocations were.

Besides polytype mixing such as 3C-SiC inclusions in the 4H- and 6H-SiC, epilayers exhibit other defects and surface features: growth pits, dislocations, micropipe, and step bunching. Growth pits are mainly caused by the initial mechanical polishing and surface

preparation. Micropipes found in epilayers are mostly propagated from the substrate surface into the epilayers. Step bunching often appears on epitaxial film grown from an off-axis low index plane in the substrates of Si, SiC and other semiconductors [94]. It is a coalescence of multiple small steps into larger steps with increased step heights. Step bunching occurs when vicinal steps become unstable under motion and come together by rearrangement. In epitaxial 4H- and 6H-SiC films, step bunching has a hill and valley like structure that is formed by the rearrangement of the surface to minimize the total surface free energy. Svyajari, et al., gave an explanation of the step bunching formation in the view of step-flow mechanism [212].

Heteroepitaxial growth of SiC over other substrates (Si, $Al_2O_3$, and TiC) has been studied for about 40 years [24, 246]. Growth systems in SiC heteroepitaxial growth are the same as for the homoepitaxy of SiC. Heteroepitaxial growth of 3C-SiC on Si substrates has been mostly studied. Si has the advantages of crystal quality, polytype control, cost, and semiconductor applications over other substrate. However, the crystal quality of heteroepitaxially grown 3C-SiC has not been good enough for electronic applications until now. The lattice constant mismatch ($a_{3C-SiC}$=4.36 Å , $a_{Si}$=5.43 Å ) and the thermal expansion coefficient mismatch (8%) between 3C-SiC and Si complicate the heteroepitaxial growth process and often produce defects of high concentration at the SiC/Si interface. Defects include dislocations, stacking faults, voids, and crystal twins. To solve these problems, a buffer-layer technique was proposed by Nishino and extensively studied by others [150]. The main idea is to grow a very thin 3C-SiC buffer layer by flowing a carbon precursor gas (such as $C_3H_8$) before the growth of a 3C-SiC film.

## *4.4 Surface Flattening of Silicon Carbide*

It is necessary to achieve a very flat SiC surface with fewer defects for the growth of an epilayer. Different methods have been used to clean and flatten polishing damages, imperfections, oxide, and contaminants on the initial SiC surface [69, 142, 175, 218, 240, 241, 243]. These methods include molten KOH or NaOH etching [243], vacuum annealing [247], sublimation etching [166], oxidation [96, 209], and high temperature etching in pure $H_2$ or $H_2$

mixtures (such as $C_2H_4$,$C_3H_8$, and HCl) [218, 240].

SiC cannot be etched by most wet chemical solutions due to its chemical inertness and hardness [69]. Molten KOH can preferentially etch defects on the SiC surfaces such as micropipes and voids, and reveal the inherent structural defects in SiC. But this method is inappropriate for SiC surface flattening [243]. Pure UHV annealing does remove contaminants and oxides, but also depletes the Si atom from the surface and leads to the surface graphitization [241]. With the removal of the graphitized film, the scratches on the surface can also be removed [71]. Other methods such as thermal oxidation followed by HF etching were also reported [209]. The above methods mentioned still cannot remove the deep scratches on the surface after polishing.

$H_2$ etching is known to be non-selective and can produce a flat SiC surface with regular steps of half to several unit cells high. It becomes the most common method to achieve flat surfaces on 4H- and 6H- SiC substrates. The next chapter will give more information about hydrogen etching effects on 4H- and 6H-SiC surfaces.

## *4.5 Summary*

SiC has more than 100 polytypes due to different stacking sequences of Si-C bilayers. Among them, 3C-, 4H- and 6H-SiC are most important because of their excellent physical and electronic properties for semiconductor applications. The bulk growth and the epilayer growth of SiC are discussed in detail concerning growth conditions and defect-related issues. The knowledge on SiC growth can help us to better understand the processes of hydrogen etching of SiC and graphitization of SiC. Hydrogen etching can efficiently flatten the surfaces of SiC wafers by the removal of scratches that are caused by mechanical polishing.

# CHAPTER V

# HYDROGEN ETCHING OF SILICON CARBIDE

Hydrogen etching has been widely used to flatten the surfaces of a SiC wafer. The flattened SiC surfaces can be the templates for later epitaxial film growth. After hydrogen etching, both the Si face and the C face of 4H- and 6H- SiC show smooth surfaces with atomic flat terraces. Surface morphology and surface components on SiC substrates are strongly dependent on chamber environment, gas components, SiC polytype (4H or 6H), face polarity (Si- or C-face), and on-axis or off-axis angles of SiC surfaces.

## *5.1 Mechanism of Hydrogen Etching*

Hydrogen etching is a non-selective method to produce smooth surfaces on 4H- and 6H-SiC substrates. Hydrogen etching removes the scratches on the top surface and produces a smooth surface with regular steps of half or several unit cells high. Chu and Campbell first reported a smooth surface on 6H-SiC after hydrogen etching [36]. Recently in situ $H_2$ etching on SiC has been investigated by several groups [28, 45, 69, 74, 112, 141, 142, 166, 178, 240, 243]. They choose different etching systems: hot-wall or cold wall, CVD chamber or simple quartz chamber, SiC-coated or -uncoated graphite susceptor, Ta strip heater or inductive heater. Besides pure $H_2$ or atomic H, several gas mixtures ($H_2$+HCl, $H_2$+$C_3H_8$, $H_2$+$C_2H_4$) are used in these systems to study the etching effect on the surface morphology of samples. The typical etching temperature range is between 1400°C and 1700°C. Etching times vary between several minutes to several hours. Typical etching rates are about 0.3-2 $\mu m$/hour. The $H_2$ etch rate increases with the rising temperature and $H_2$ flow rate. 4H-SiC is more rapidly etched than 6H-SiC. On-axis SiC is more rapidly etched than off-axis SiC [240].

The reaction of SiC with $H_2$ at high temperatures (above 1400°C) results in the gaseous hydrocarbon ($CH_4$,$C_2H_2$) and elemental silicon byproducts [69]. The vapor pressure of hydrocarbon is higher than that of evaporated Si ($10^{-6}$ to $10^{-5}$ torr [28]). Consequently,

the Si atoms condense on the surface and become droplets. For example, after pure $H_2$ etching at atmospheric pressure in a SiC-coated graphite susceptor, Si droplets were found on the SiC surface, preferentially near the defects or step edges, or uniformly distributed over the whole surface [28]. In general, Si droplets are more prominent on 4H-SiC surfaces than on 6H-SiC surfaces. These droplets are not from the SiC coated susceptor, but from the SiC substrates themselves. To suppress the evaporation rate of hydrocarbon, an overpressured hydrocarbon environment is maintained in the chamber, either by using a uncoated graphite susceptor or by adding an amount of hydrocarbon gases ($C_3H_8$, $C_2H_4$) diluted by $H_2$. (The former produces hydrocarbons by the reaction between $H_2$ and uncoated graphite.) The amount of hydrocarbons affects the etching rate of SiC and the final surface morphology [28, 227]. An alternative way is to remove in situ Si droplets by HCl diluted in $H_2$, leaving gaseous chlorosilanes. The HCl concentration and the etching temperature also affect the final surface morphology [240]. Another way is to increase the evaporation rate of Si by reducing the ambient pressure [28]. However, excessive HCl etching causes the surface roughness and etch pits [28, 240]. The rapid etching rate of SiC by reducing the ambient pressure could also reveal etch pits [28]. Hartman, et al., reported a different pure hydrogen etching result using a simple system with a Ta strip heater [74]. They did not find Si droplets under AFM. And they attributed the absence of Si droplets to the residual oxygen in the chamber that would oxidize the excess Si leading to its removal.

In theory, the mechanism of hydrogen etching on SiC has been studied from equilibrium thermodynamic calculations [74]. For the potential reactions during the hydrogen etching on 6H-SiC (0001) surface, changes of free energies of formation/reaction were calculated by the HSC chemistry software [74]. Data show the possible reactions between molecule hydrogen and SiC give positive values in free energy change. While, the possible reactions between atomic hydrogen and SiC give negative values in free energy change when the $SiH_4$ and/or hydrocarbon are the reaction products. Moreover, after $H_2$ etching above 1100°C, dangling bonds on the surface were terminated with atomic hydrogen [196, 221]. From experiments, Harris, et al., attributed the increase of etching rate of SiC in susceptors constructed of molybdenum, tantalum, tantalum silicide to their catalytic action in the dissociation of

molecule hydrogen [73]. Losurdo reported that clean, atomically ordered, smooth surfaces with terraces were produced on both 6H- and 4H-SiC (0001) surfaces after the reaction of atomic hydrogen plasma etching at 200°C [112].

All these indicate the necessity of atomic H presence during the $H_2$ etching on SiC. The $H_2$ etching process can be pictured as the enhanced dissociation of molecular hydrogen at high temperature, the subsequent reaction of atomic hydrogen with the silicon via the gaseous silane formation, and remove the carbon via gaseous hydrocarbon formation [74, 178]. The free silicon can also be removed via direct evaporation.

## *5.2 Experiment Equipment and Procedure*

### 5.2.1 Design of the Hydrogen Etching System

A home-made hydrogen etching system is designed and assembled to operate in a temperature range of 1400-1650°C with a $H_2$/Ar mixed gas flowing under one atmospheric pressure. The system consists of an induction heating RF power supply, an etching chamber, a thermocouple, a hydrogen gas flowing system, a high vacuum system with pressure gauges, and a PC to record and modulate the temperature through the Labview interface. Figure 5.1 gives the schematic diagram of this hydrogen etching system.

A 2kW Hotshot induction RF power supply is provided by Ameritherm Inc. The power supply has an extended remote heat station with a RF coil.

The etching chamber is sealed by an one-end, single-wall Pyrex glass tube. The bottom open end of the glass tube is tightly sealed to a steel base stand by a rubber O-ring. The air-cooled etching chamber is aligned vertically and the heating hotzone region is surrounded by the RF coil.

From the outer to the inner, the hotzone region inside the etching chamber consists of a thick alumina hollow cylinder for thermal shield, a Mo metal source to be RF heated, another thin, long, and hollow alumina tube as the gas flow channel, and a thin Ta sheet to protect the SiC samples from sidewall contaminations. A sample holder made of Ta is used to hold SiC samples in the center of the heating zone. A $H_2$/Ar mixture flows across the surfaces of a SiC sample upward through the inner alumina tube. A Ta cap loosely covers

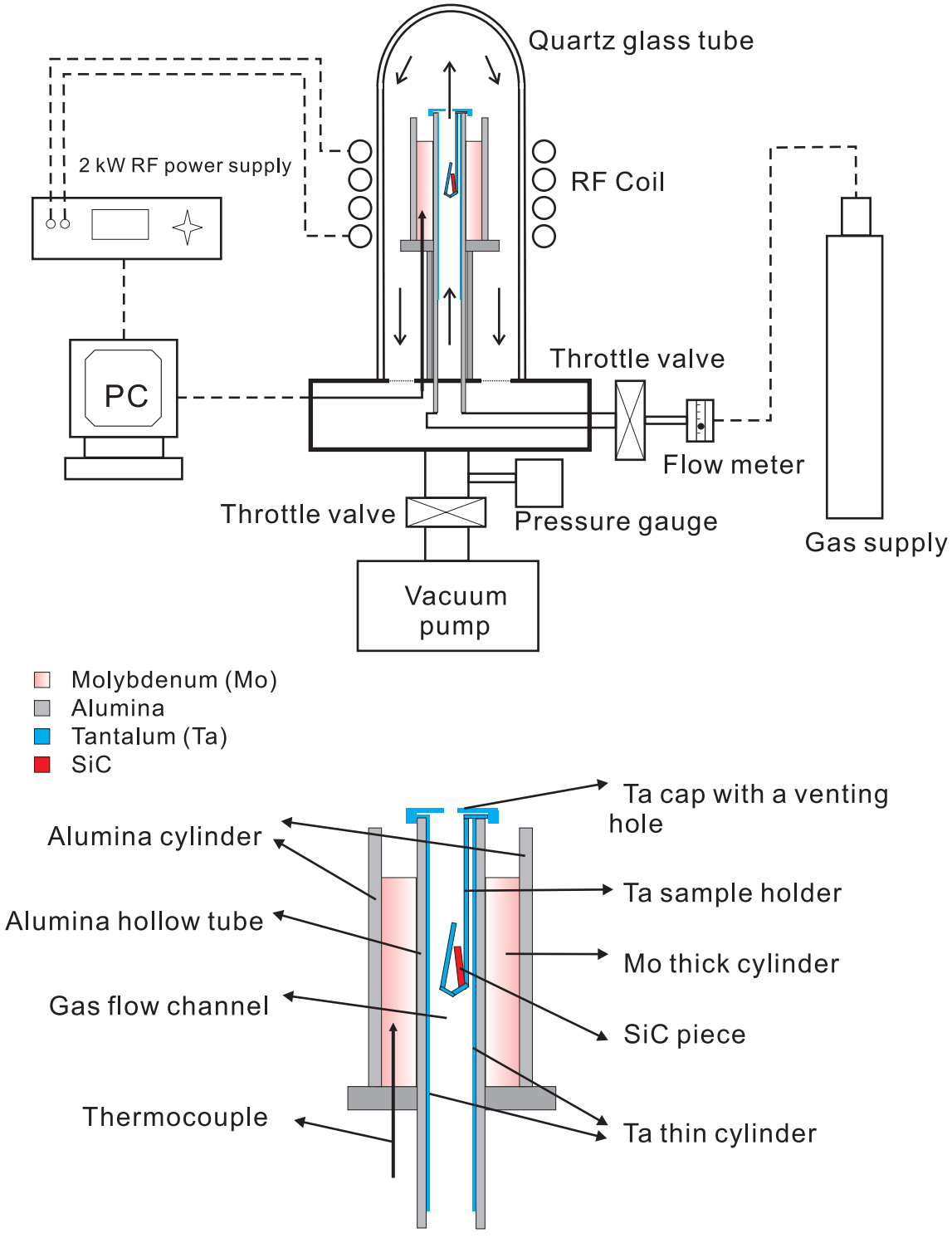


**Figure 5.1:** Schematic diagram of hydrogen etching system.

the top end of the inner alumina tube for two purposes. One is to reduce the possible contamination deposition of byproducts on SiC surfaces; the other one is to leave sufficient space for byproducts to flow out of the etching chamber. The SiC sample is heated by thermal radiation from the Mo source that is inductively heated by the RF coil.

A pair of thermocouple wires are bonded at one end and positioned inside the Mo metal source to approximately measure the etching temperature on the SiC sample. The other ends of wires are located far away from the heating zone so that the reference temperature is very close to room temperature. An optical pyrometer is used to measure the temperature on the top surface of the Mo metal source. The temperature reading difference between the thermocouple and the pyrometer is within 50°C int the typical etching temperature range of 1450-1600°C.

A mixture of 5% hydrogen and 95% argon is stored in a gas cylinder suppied by South Airgas. The mixture is driven by the pressure difference between the gas cylinder and the gas outlet of the etching chamber.

The residual air in the etching chamber is pre-evacuated by a turbo-pump and a mechanical pump. An ion gauge is used to monitor the pressure in the chamber. The turbo-pump and the heat station of the power supply system are water cooled.

Finally, connected to the whole system is a computer that can remotely record the etching temperature from the thermocouple and modulate the output power by a standard PID control. A Labview program is written to control communications between the computer and the whole etching system through a DAQ board.

### 5.2.2 Sample Preclean and Etching Experiment Procedure

Except for one SiC wafer from NASA, other SiC wafers were bought from Cree Inc. SiC wafers are categorized by polytypes (4H- or 6H- SiC), polarity (Si-face, C-face, or both), on-axis or off-axis, doping or insulating, and quality grade. Table 5.1 summarizes all the wafers obtained from NASA or Cree Inc. Most wafers are used for both hydrogen etching experiments and graphitization experiments.

As received SiC wafers have randomly distributed scratches on the surfaces, as deep as

**Table 5.1:** The list of SiC wafers.

| Wafer No. | Received Date | Poly-type | Specification | Grade | Orientation (°) | Resistivity $\rho$(Ω-cm) |
|---|---|---|---|---|---|---|
| NASA | - | 6H | Si face, mesas | - | - | |
| B | - | 6H | Si face, big off-axis | - | - | |
| 1 | - | 6H | Si face; irregular | - | - | |
| 2 | 2004/07 | 6H | Si face | P | 0.09 | 0.209 |
| 3 | 2004/06 | 4H | Double face; Si epi | R | 0.12 | ≤1E5 |
| 4 (400 series) | 2005/08 | 4H | Double face, Si epi | R | 0.14 | ≥1E5 |
| 5 (600 series) | 2005/09 | 4H | Double face; Si epi | R | 0.02 | ≤1E5 |
| 6 (700 series) | 2006/09 | 4H | Double face; C epi | R | 0.2 | ≥1E5 |
| 7 (800 Series) | 2007/12 | 4H | C face CMP polish | R | 0.06 | ≤1E5 |
| 8 | 2005/12 | 6H | Double face; Si epi | R | 0.2 | 0.059 |

tens of nm, and as long as several hundreds of $\mu m$. Before any treatment, SiC wafers were diced typically into 3.5 mm × 4.5 mm pieces along certain crystal orientations.

In a typical hydrogen etching procedure, one SiC piece is cleaned ultrasonically with acetone, ethanol for about 10 mins, respectively, and blown dry with nitrogen. This piece is placed on the Ta sample holder and transferred in air to the hydrogen etching chamber. The residual air in the whole system is pumped down to $10^{-6}$ torr before being RF heated.

Four heating stages are involved in a typical etching process: pre-baking, rising, etching, and cooling. Figure 5.2 shows a typical heating cycle for this process. The temperature history chart and the corresponding power history chart are recorded simultaneously. The RF power is automatically PID regulated to meet the settings of the rise/cooling rates and the final etching temperature.

At the beginning, a SiC piece is pre-baked at around 200°C for 10-30 mins. During this period, residual air and water vapor are heated up and pumped out of the chamber. At the end of this stage, the etching chamber is isolated from the pumping system by a throttle valve. Meanwhile, the mixture of 5% hydrogen and 95% nitrogen is filled into the etching chamber at a flow rate of 200 sccm. When the gas pressure is above 1 atm pressure, the gas outlet throttle valve opens. The gas flows upwards inside the inner alumina tube, then out of the chamebr from the outlet.

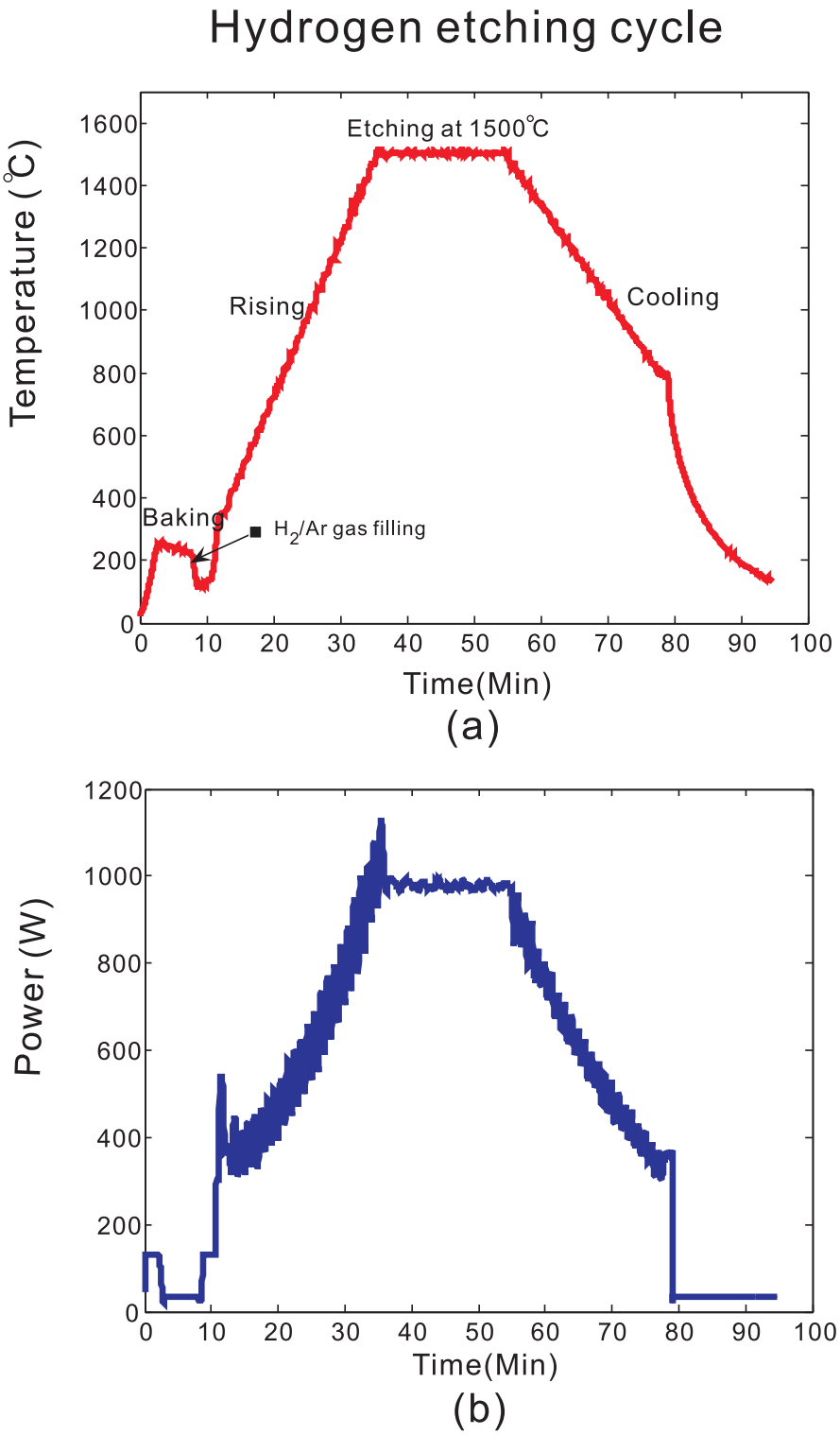


**Figure 5.2:** Hydrogen etching cycle over time. (a) Temperature as a function of time. (b) RF power as a function of time. RF power is PID adjusted to meet the temperature settings.

During the rising stage, the SiC piece is gradually heated up at a rate of 50-100°C per minute. When the temperature reaches the final etching temperature (typically 1450-1650°C), the SiC piece will be heated for 15-60 mins. The flowing gas removes byproducts of reactions out of the chamber. After etching, the temperature ramps down to 800°C at a rate of 100°C per minute, then naturally cools down to room temperature.

## *5.3 Result and Discussion*

SiC samples are characterized by atomic force microscopy (AFM) before and after hydrogen etching. The morphology of SiC surface does not change until the etching temperature is high enough (above 1450°C) to trigger the reactions between SiC and hydrogen. Systematic experimental results manifest that surface morphology of SiC varies with polytype, face polarity, off-axis angle, and the bulk crystal quality.

### 5.3.1 On-axis and Off-axis 6H-SiC

Most studies on 6H-SiC were done on the Si face (0001). Three kinds of 6H-SiC wafers have been studied. (wafer 1, 2, NASA, and B (with a big off-axis angle) from Cree Inc.)

Figure 5.3 gives the morphology change on the Si face of 6H-SiC with temperature. Figure 5.3(a) reveals many scratches on the surface of an as-received SiC sample piece. These scratches, as deep as 10 nm, are distributed randomly on the surface. As the etching temperature increases, the scratches begin to blur then disappear, as seen in Figure 5.3(b)-(c). After these scratches are removed by $H_2$ etching, the surface shows atomic flat terraces of 200 - 300 nm wide (Figure 5.3(d)). The height between adjacent terraces is typically either 0.75 nm or 1.5 nm, corresponding to half or one unit cell height (1.5 nm) of 6H-SiC. The uniform step height along terraces indicates that identical stacking sequences of Si-C bilayers on the terraces.

Hydrogen etching is believed to occur at the step edges where there are more defects and dangling bonds, and to extend along the plateaus of each terrace [45]. The vertical etching rate on the terraces is very slow so that a longer etching time does not produce a higher step between terraces.

Equidistant step structures have been studied both energetically and kinetically [161].

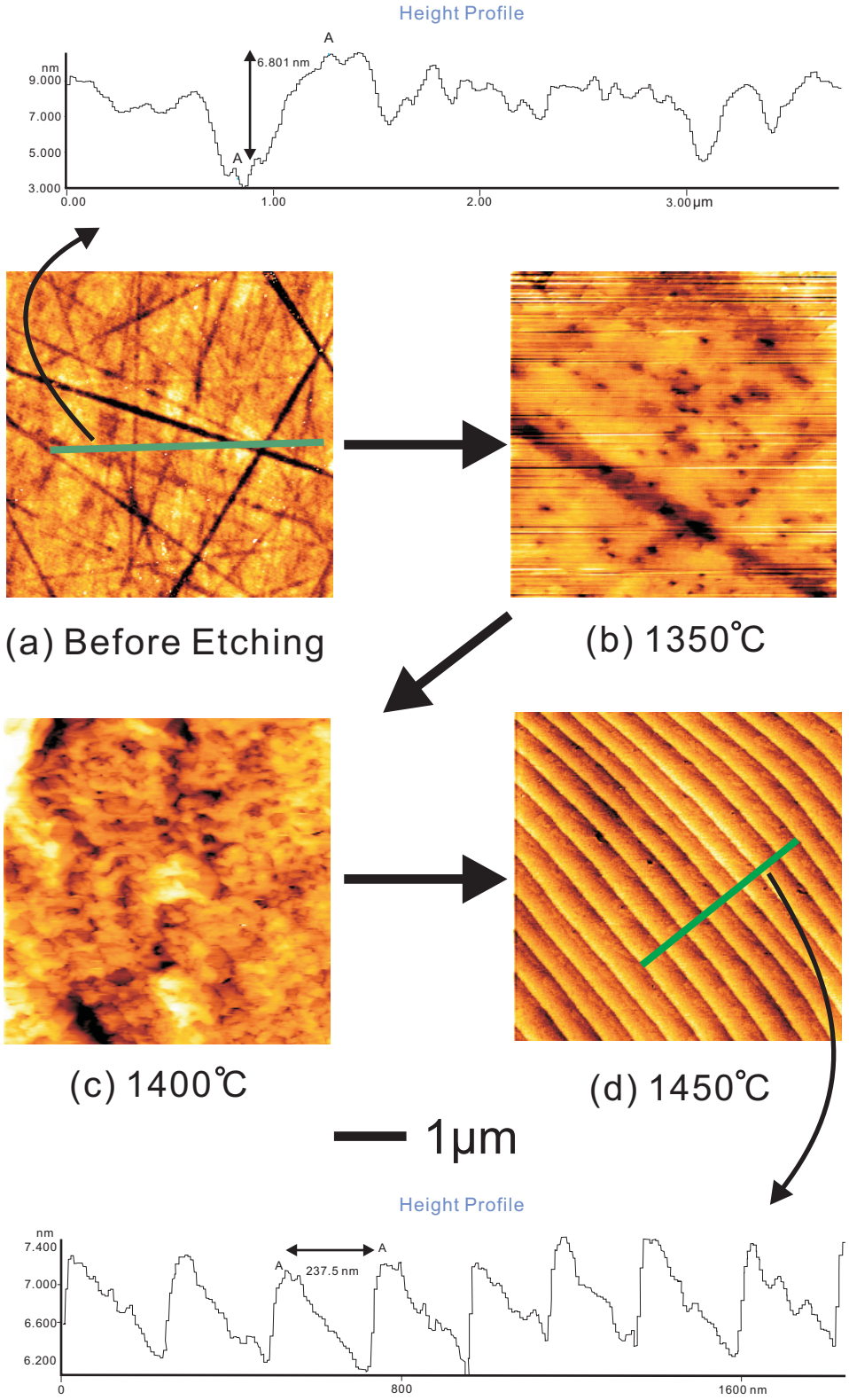


**Figure 5.3:** Morphology changes with elevated hydrogen etching temperature on the Si face of 6H-SiC.

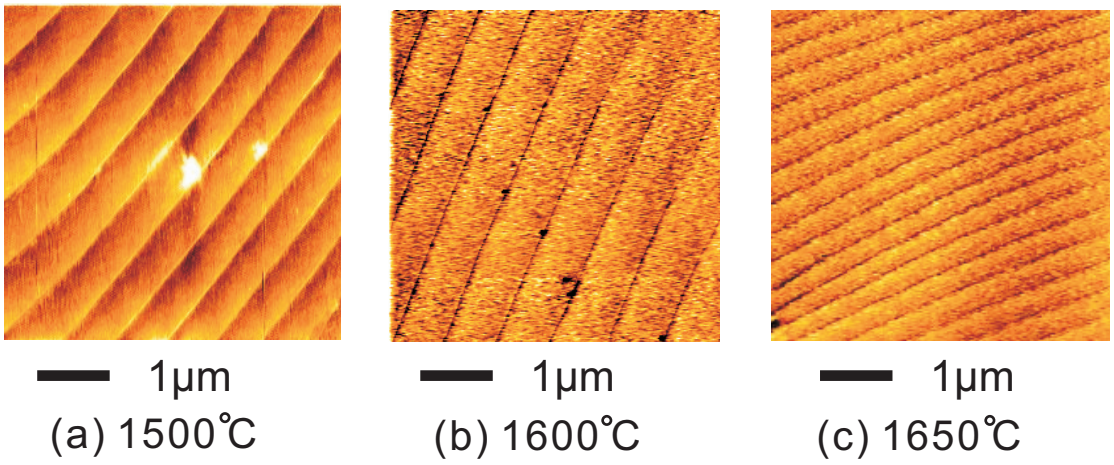


**Figure 5.4:** AFM images of three etched 6H-SiC samples (from SiC wafer No.1). (a) Sample A (etched at 1500°C for 20 mins). (b) Sample B (etched at 1600°C for 20 mins). (c) Sample C(etched at 1650°C for 20 mins).

The most possible mechanism is step repulsive interaction through the minimization process of total surface energy [161]. A mechanism of asymmetrical step kinetics [190] was also proposed to explain the equidistant step structures and the step bunching of macrosteps. The competition between the mechanism for equidistant step structures and the mechanism for step bunching allows various stepped morphology.

On the Si face (0001) of 6H-SiC, the average width and step height of terraces do not have a clear correlation with hydrogen etching temperature and time. Experiments have been repeated over a broad etching temperature range (1450-1650°C) and a broad etching time range (15 mins to 2 hrs). Etching at a higher temperature for a longer time do not cause a significant extension of the average terrace width, and on the whole, do not affect much the surface morphology. Figure 5.4 shows AFM images from three 6H-SiC samples that are etched individually at three different temperatures for a fixed etching time.

The average terrace width and step height are determined mainly by the off-axis angle of a SiC wafer. The wafers (No.1, 2, and NASA) with smaller off-axis angles produce wider terraces. The wafer No.B with a big off-axis angle (3.25 degrees) produces much narrower terraces that are hardly recognized under AFM (Figure 5.5). Similar results were also observed by Xie et al. [240]. Off-axis SiC with several vicinal angles (3.5-8 degrees) was studied by Nakagawa et al. [140]. They observed nanofacets of (0001) and $(11\bar{2}n)$

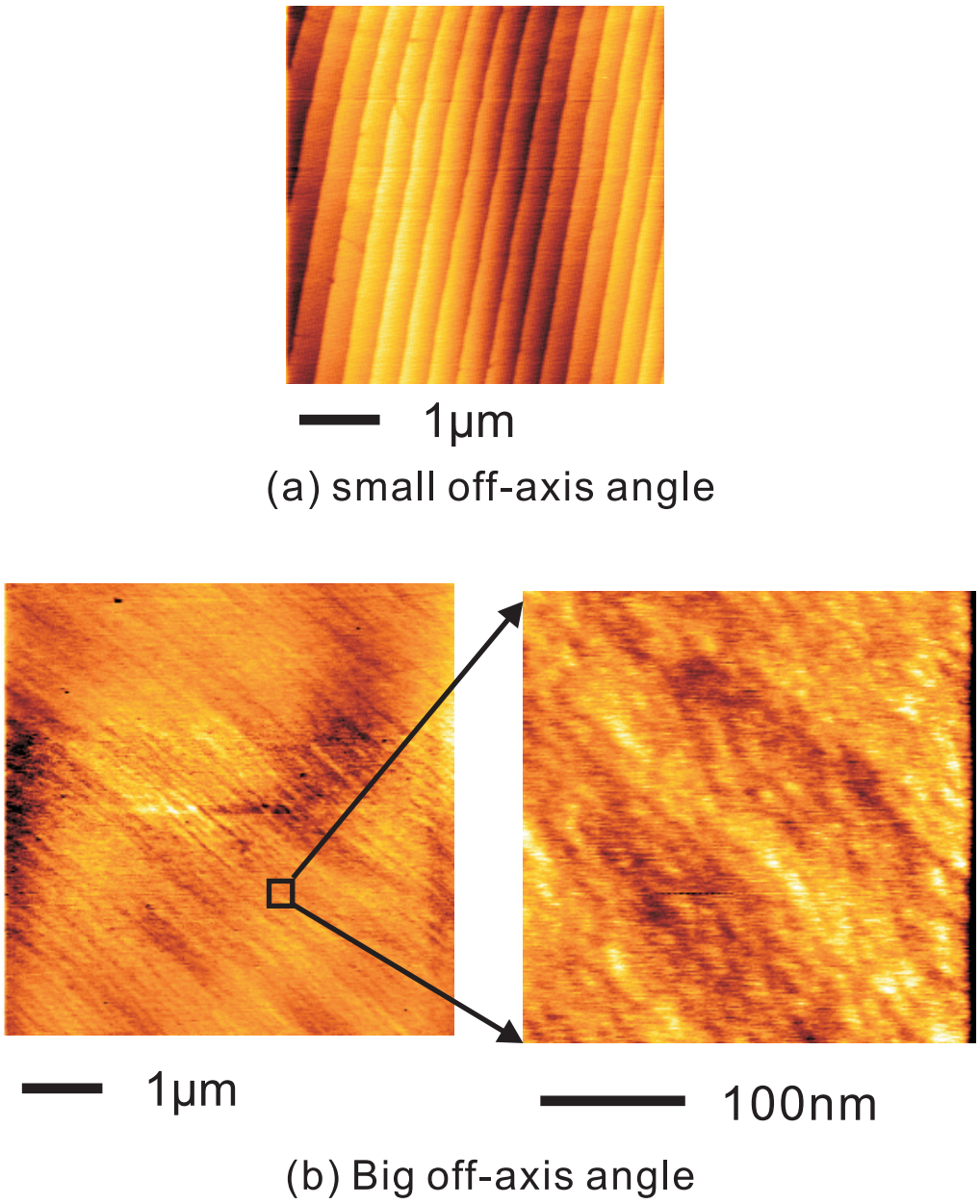


**Figure 5.5:** AFM images on 6H-SiC wafers with different off-axis angles. (a) Wafer No.2 (0.09 degrees off-axis angle). (b) Wafer No.B (3.25 degrees off-axis angle).

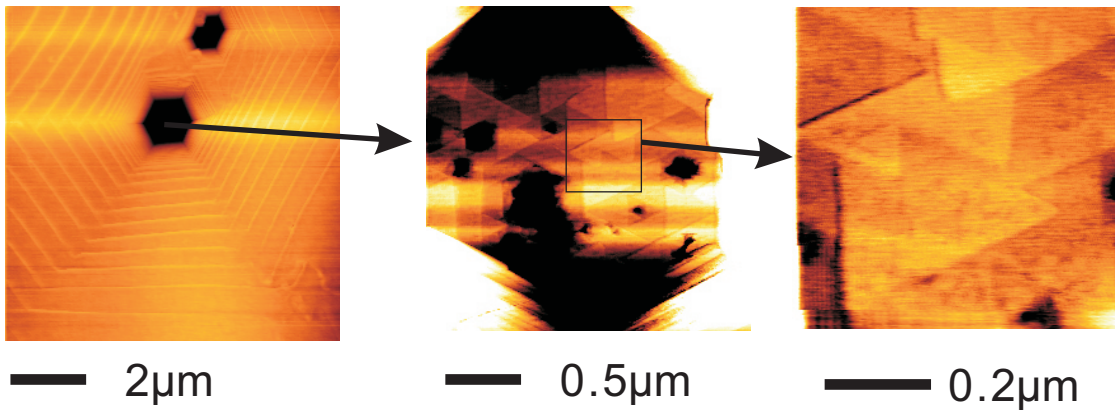


**Figure 5.6:** Hexagonal etch pits on the 6H-SiC surface.

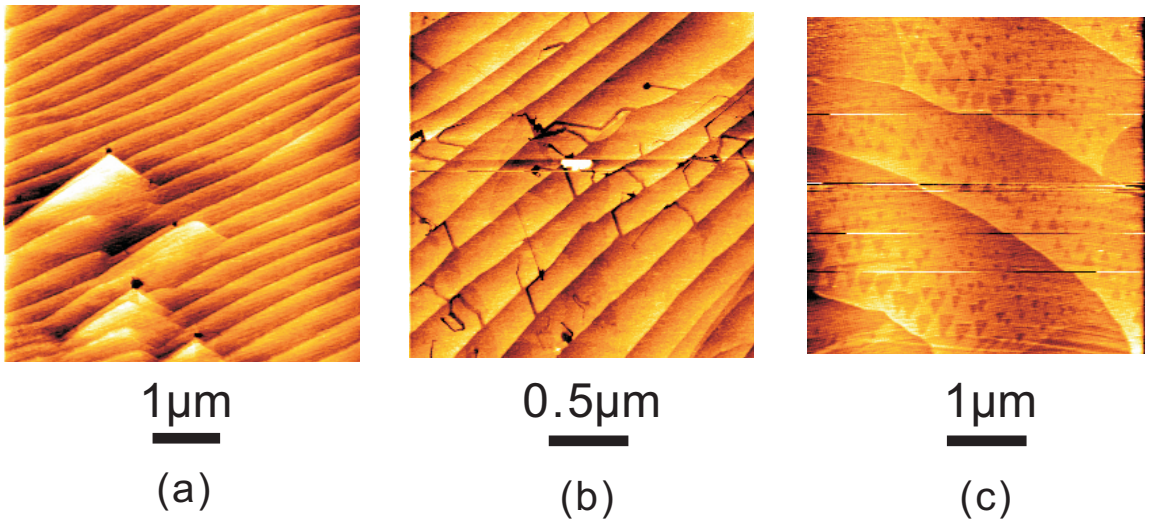


**Figure 5.7:** Other defects on etched 6H-SiC surface.

in a nanometer scale on cross sectional high resolution transmission electron microscopy (HRTEM) images. The self-ordering mechanism of nanofaceting on vicinal SiC surfaces was explained in terms of surface free energy and surface elasticity theory.

Besides hydrogen etching parameters, the morphology of 6H-SiC depends on the crystal quality and defects on the surface. Figure 5.6 shows hexagonal etch pits with terrace arrays around them after hydrogen etching. Inside the holes, many triangular shaped structures are observed on the bottom, overlapping each other. The hexagonal pattern hole originates from a screw dislocation or a micropipe [74, 79]. Hydrogen etching behavior in the interior of hexagonal voids was studied by Sander et al. [188]. They found that a preferential removal of C inside the voids leaded to a pure Si surface at the bottom of the voids.

Figure 5.7 shows other kinds of etch pits. Some defects are pinned at the bunched steps as shown in Figure 5.7(a). Etch pits easily appear where terraces are crossed with each other. Some tube-like defects are observed on some locations of a sample, and these defects are possibly attributed to the crystal qualify of the bulk SiC. Figure 5.7(c) reveals some very small triangular pits as deep as 0.5 - 1.0 nm. The possible tip effect of AFM cantilever on the image quality cannot explain that because most AFM images do not reveal these highly resolved features. The reason for the appearance of these triangular pits is unclear. It may be caused by the imbalance of the Si/C etching rate ratio on the surface.

### 5.3.2 On-axis 4H-SiC

Both the Si face and the C face of 4H-SiC have been hydrogen etched and characterized by AFM. Mechanical scratches on the as-received 4H- SiC wafers (No.3-7) are quite like those on 6H-SiC. For the normally polished 4H-SiC wafers (No.3 and 5), scratches can be as deep as 10 nm. Figure 5.8(a)-(b) show surface morphologies on the Si face and C face of a 4H-SiC wafer (No.3) before hydrogen etching. For higher-quality, fine-polished 4H-SiC wafers (No.4, 6, and 7), the depth of scratches is typically within 2 nm.

The surface morphology on etched 4H-SiC is dependent on polarity (Si or C face), polytype (4H or 6H), and wafer crystal quality. First I will compare the Si face with the C face on 4H-SiC wafers. Later I will compare 4H-SiC with 6H-SiC on the Si face. Even for the same polytype, different crystal quality SiC wafers show slightly different surface morphologies after etching.

Figure 5.8(c)-(d) exhibit AFM images taken on one 4H-SiC sample (221) from wafer No.3 after hydrogen etching. The Si face and C face of this sample are hydrogen-etched simultaneously under the same conditions. After etching, both faces show flat terraces, and the surface roughness is less than 2 nm. Compared with the Si face, more uniform terraces are seen on the C face. The terrace step height on the C face is mostly about 1-2 nm, and the widths of terraces are in the range of several hundreds nm to about 2 $\mu m$.

For higher crystal quality 4H-SiC wafers (No.4, 6, and 7), more regular terraces are seen on both surfaces with fewer defects. Figure 5.9(a)-(d) show AFM images taken on

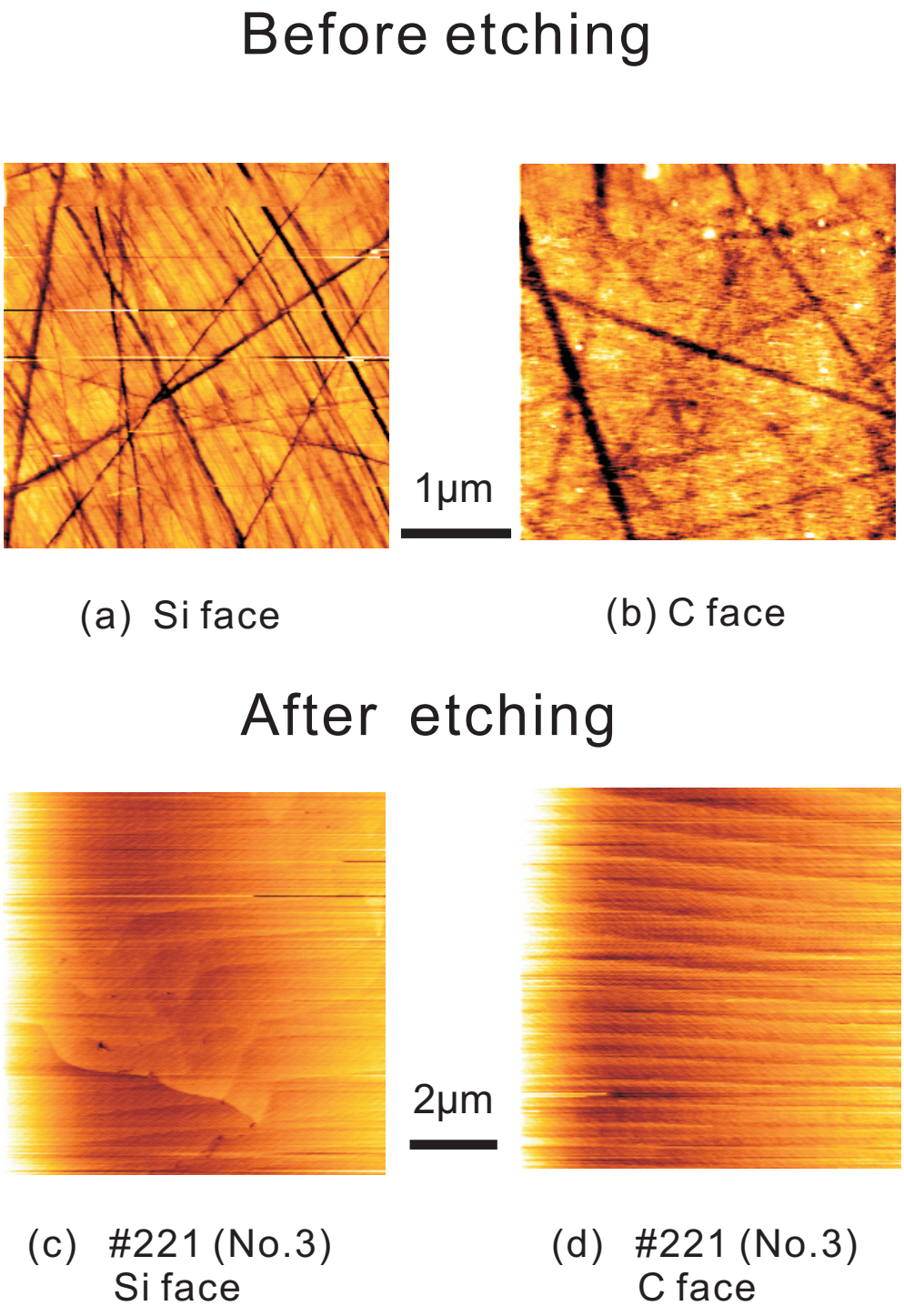


**Figure 5.8:** AFM images on the Si face and the C face of a 4H-SiC wafer (No.3). Before etching: (a) Si ; (b) C face. After etching(1650°C for 30 mins): (c)Sample 221, Si face; (d) Sample 221, C face.

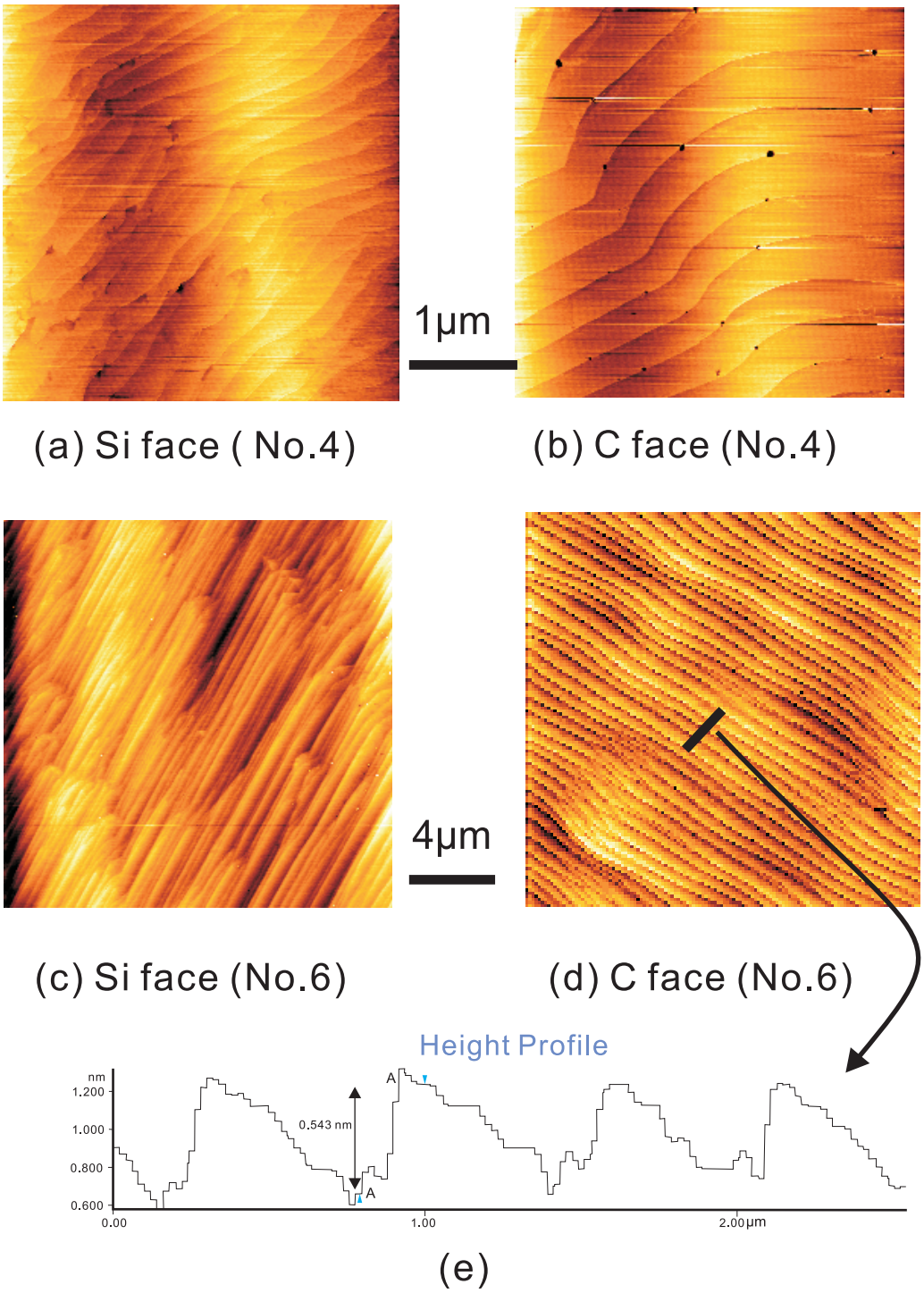


**Figure 5.9:** AFM images on high quality 4H-SiC wafers (No.4 and No.6) after hydrogen etching at 1550°C for 30 mins. (a) Si face (No.4) . (b) C face (No.4). (c) Si face (No.6). (d) C face (No.6). (e) Height profiles of terraces on (d).

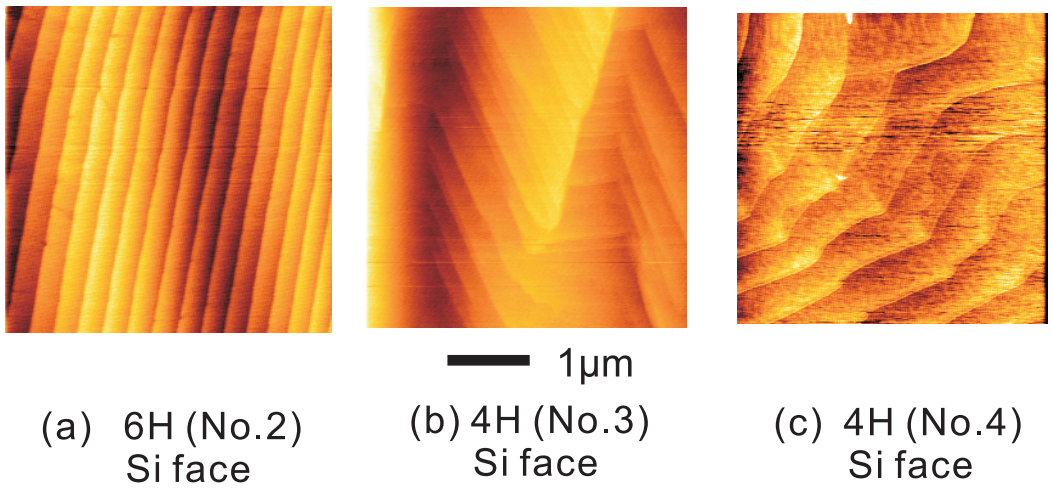


**Figure 5.10:** AFM image comparison between on-axis 6H-SiC and on-axis 4H-SiC. (a) 6H, Si face (wafer No.2). (b) 4H, Si face (wafer No.3). (c) 4H, Si face(wafer No.6).

etched SiC samples from the No.4 and No.6 wafers, respectively. These images show quite uniform terraces with slight local undulations caused by defects and/or thermal-driven surface movement. The step height between terraces is typically between 0.5 nm and 2 nm. The height profile on the C face of the No.6 wafer is given on Figure 5.9(e). The step height between adjacent terraces is about 0.5 nm that is corresponding to half of unit cell height of 4H-SiC.

The surface morphology of etched SiC wafers depends not only on polarity (Si or C face) but also on polytype (4H or 6H). Here I compare the surface morphologies on the Si face between on-axis 6H-SiC and on-axis 4H-SiC. The On-axis 6H-SiC shows a smooth surface with uniformly distributed terraces (see Figure 5.10(a)). The On-axis 4H-SiC shows undulated or zigzag-like terraces on the surface. For poor quality 4H-SiC wafers (No.3 and 5), more defects or trigonal protrusions are found on the surface (see Figure 5.10(b)). These protrusions are possibly attributed to the extended stacking faults [69]. High-quality 4H-SiC wafers (No.4, 6 and 7) have more regular terraces with fewer protrusions (see Figure 5.10(c) and Figure 5.9(a), and (c)).

On the whole, there are slight surface morphological differences between the Si face and the C face of 4H-SiC in terrace shape, step height, and terrace distribution uniformity.

Terraces on the Si face of 4H-SiC are not as regular as those on the 6H-SiC. Higher crystal quality 4H-SiC wafers can reduce the above differences. These phenomena have been observed by other groups [69, 178].

## *5.4 Summary*

Hydrogen etching can achieve smooth surfaces on both faces of 4H- and 6H-SiC wafers. The surface morphology of SiC is determined by not only hydrogen etching parameters but also other factors related to a SiC wafer itself. The main facts observed in the experiments are summarized below.

- As-received SiC wafers from Cree Inc. have mechanical scratches on the surfaces. The depth of scratches depends on how the surfaces are polished. The depth height of scratches varies from several to 10 nm for normal polished wafers (No.2, 3, and 5) and within 2 nm for fine-polished SiC wafers (No.4, 6, and 7).

- Hydrogen etching on 4H- and 6H-SiC eliminates mechanical scratches on the surfaces and achieve smooth surfaces with atomic flat terraces. The step height between terraces is in the range of half to several unit cells high of SiC polytypes.

- Straight and regular terraces are achieved on the Si face of 6H-SiC. Terrace width is determined by the off-axis angle of the SiC wafer. A big off-axis 6H-SiC wafer has much narrower terraces than a small off-axis SiC wafer.

- Flat terraces are achieved on 4H-SiC wafers, although slightly different from those on 6H-SiC. Compared with the Si face of 4H-SiC, the C face of 4H-SiC has more regular terraces with fewer defects. The surface morphology difference between the Si-face and the C-face diminishes for higher quality 4H-SiC wafers.

# CHAPTER VI

# GRAPHITIZATION OF SILICON CARBIDE

This chapter describes how to grow high quality multilayer (single to tens of layers) epitaxial graphene on 4H- and 6H-SiC in a homemade RF vacuum furnace. Epitaxial graphene films are characterized by Atomic Force Microscope (AFM), Auger Electron Spectroscopy (AES), Low Energy Electron Diffraction (LEED), High Resolution Transmission Electron Microscope (HRTEM), Scanning Tunneling Microscope (STM), and X-ray scattering.

## *6.1 Mechanism of SiC Graphitization*

4H-SiC and 6H-SiC are chosen as the substrates on which to grow epitaxial graphene films. The graphitization of SiC has been studied since the bulk SiC crystal growth method was invented by Lely in 1955. SiC graphitization was regarded originally as a big problem of inducing defects during the sublimation growth of SiC crystal boules (see Chapter IV). Later, surface scientists explored the complicated surface reconstructions involved in the SiC graphitization in an ultrahigh vacuum (UHV) environment ($10^{-10}$ Torr). As seen later, our high-quality, epitaxial graphene films can grow on 4H- and 6H-SiC substrates in a fairly low vacuum environment. we find that graphene layers grown on the C face are stacked rotationally over each other, which preserves the Dirac properties of single-layer graphene.

### 6.1.1 Graphitization in UHV

The UHV environment protects SiC substrates and the later graphene layers from oxidation. The crystal structure and surface morphology can be in situ analyzed by LEED, AES, STM, and other techniques.

SiC experiences a complicated surface reconstruction process before the first graphene layer grows on the top. The description of surface reconstruction follows. The environment of surface atoms considerably differs from that of the bulk atoms inside the crystal. For example, surface atoms with unsaturated or dangling bonds can rearrange themselves or

bond with adatoms, which leads to surface reconstruction (periodic surface rearrangement). The reconstruction is generally described by the notation of (m×n)$R_{\varphi}$, with m and n being respective multiples of the two lattice vectors in the unreconstructed bulk-like surface. The rotation angle $\varphi$ indicates the rotation of the superstructure lattice relative to the bulk lattice.

Surface reconstruction and graphitization on the hexagonal SiC surface (0001) have been studied by AES, LEED, STM, X-ray photoemission spectroscopy (XPS), and electron energy loss spectroscopy (EELS) in an ultra high vacuum (UHV) system ($10^{-8}$ -$10^{-10}$ Torr) by many groups [31, 51, 74, 80, 112, 117, 167, 168, 183, 184, 224, 239, 241]. When a $H_2$ etched SiC sample is transferred to a UHV chamber via air, a highly ordered monolayer of silicon dioxide is grown on the top of SiC surfaces, as observed by Bernhardt et al.[22]. After thermal annealing at around 1000°C [74, 166], oxygen is evaporated from the surface in the form of a volatile SiO compound, which leaves the SiC surface depleted of Si. On the Si face of hexagonal SiC, a $\sqrt{3} \times \sqrt{3}$ R30 reconstruction LEED pattern is typically achieved at a temperature near 1100°C [166]. A structural model of Si or C adatoms in threefold symmetric sites was accepted as the atomic configuration for this reconstruction even though the model still had problems in explaining some experimental findings [119]. Annealing treatment on SiC for the development of the $\sqrt{3}\times\sqrt{3}$ R30 reconstruction does not significantly influence the surface morphology [166]. Upon a higher temperature annealing, the $\sqrt{3} \times \sqrt{3}$ R30 reconstruction transforms to $6\sqrt{3} \times 6\sqrt{3}$ R30 reconstruction with the depletion of more Si atoms.

On the C face of hexagonal SiC, the surface reconstructions before the formation of the first graphene layer have not been well understood [8, 51, 53, 80, 108, 138]. In the previous work done by Dr. Tianbo Li in the group of Prof. Phillip First, a $\sqrt{3} \times \sqrt{3}$ R30 reconstruction LEED pattern is typically observed on a $H_2$ etched SiC sample before graphitization [109]. In agreement with Starke, et al., Li attributes the $\sqrt{3} \times \sqrt{3}$ R30 reconstruction to a silicate monolayer that covers the surface of the C face. He also finds that the SiC patterns change from SiC $\sqrt{3} \times \sqrt{3}$ R30 to SiC 1×1, then disappear when more graphene layers grow. Neither SiC $6\sqrt{3} \times 6\sqrt{3}$ R30 nor any double scattering LEED

patterns appear at any phase. Li claims that either no interfacial layer exists between graphene layers and the SiC substrate or the interfacial layer is thin and disordered [109]. Li also observes SiC 3×3 reconstruction after the UHV annealing at 1150°C, a temperature below the graphitization temperature.

The specific formation mechanism of initial graphene layer and the interface states are still being investigated by different groups [51, 138, 184, 185]. A simple and acceptable picture is given below. When excess Si atoms are evaporated away from the top surface, C atoms that are left on the top three layers start to collapse and reconstruct into one graphene layer with a honeycomb lattice structure [224]. With the increase of temperature and/or time, more graphene layers grow upwards from the interface between SiC and grown graphite layers [51, 224].

Due to the different atomic structure on the Si face (0001) and the C face ($000\bar{1}$) of 4H- and 6H-SiC, one would expect different graphitization processes for these two basal faces that are graphitized under identical conditions. Graphene layers on the Si face of 6H-SiC were claimed by others to be characteristic of layer by layer, unconstrained, epitaxial single crystalline quality with a very low mosaicity and good homogeneity [31, 52, 224]. Graphene layers grown on the C face of 4H- and 6H- SiC were claimed by others to be azimuthally disordered [53, 138]. On the C face, a significant fraction of the graphene layers still keeps a preferred orientation that the graphene lattice basis vectors are rotated by 30 degrees with respect to the basis vector of the SiC lattice [224, 53]. The graphite film on the C face is viewed as a mosaic of small crystalline domains with azimuthal disorder. Each graphite domain is azimuthally disordered to each other. When the graphite layers grows across boundaries of individual domains, the grown layer may be lifted up at domain boundaries. As a result, the scroll- or tube- like structures begin to form [8, 138]. Derycke, et al., claimed that single-wall carbon nanotubes were found on the Si face of 6H-SiC at temperatures above 1500°C, and these nanotubes were preferentially in the directions parallel and perpendicular to the steps of SiC terraces [41]. Different from above observations and explanation, graphene layers grown on the C face of 4H-SiC in our homemade RF vacuum

furnace (instead of UHV) are rationally stacked over each other as testified by X-ray reflectivity experiments [75, 76]. Different from Derycke, et al.'s findings, pucker-like structures are observed on epitaxial graphene film on the C face. These pucker-like structures are possibly caused by the thermal contraction between the SiC substrate and graphene layers and/or the presence of sharp edge boundaries of SiC terraces.

### 6.1.2 Graphitization in a High Vacuum Induction Furnace

The demanding UHV environment is prohibitive for the commercial application of SiC graphitization. In fact, SiC graphitization can be realized in a fairly low vacuum system. To understand the role of residual air in the SiC graphitization, possible reactions between oxygen and SiC in different gas environments and pressure ranges are worthy of mention.

The reactions of oxygen with the 4H- and 6H-SiC have been studied at different temperatures (200-1800°C) under different partial $O_2$ pressure ranges ($10^{-8}$ Torr to 1 atm) [4, 60, 66, 72, 96, 177, 189, 203, 204, 226]. At a high partial $O_2$ pressure and a high temperature, SiC surfaces are oxidized with the formation of a $SiO_2$ layer and a weight gain of the SiC sample, which is called passive oxidation [66]. The dominant reaction of passive oxidation is $2SiC + 3O_2 = 2SiO_2 + 2CO$ [72, 177]. The $SiO_2$ layer hinders the diffusion of $O_2$ deep into the SiC underneath. Passive oxidation gradually transits to active oxidation at lower $O_2$ pressures and higher temperatures. Active oxidation is characteristic of vaporization of SiO and CO and a weight loss of the sample. The dominant reaction is $SiC + O_2 = SiO + CO$ [66, 177]. SiC oxidation in CO-$CO_2$ gas mixtures also shows the passive to active transition when the pressure ratio of $P(CO_2)/P(CO)$ decreases [60, 195]. All these show that oxygen not only can passively oxidize the SiC but also can actively etch away SiC, dependent on the partial $O_2$ pressure, temperature, etc. If the surface of SiC can be protected from the active oxidation, it is possible to graphitize the SiC in even a low vacuum environment.

Graphitization of SiC in a vacuum system with residual air at high temperature was studied by Kusunoki's group in Japan [98, 99, 101, 102, 100, 103]. In their experiments, SiC wafers were heated at different temperatures (1300C-1800°C) for half an hour in a vacuum

furnace ($1\times10^{-4}$ Torr) with an electric resistance carbon heater. The heating rate was 15°C/min. At 1700°C, well aligned carbon nanotubes (CNTs) were formed perpendicular over the C face of SiC and thin graphite layers were formed epitaxially on the Si face of SiC [100]. The graphite layer grown on the Si face was explained using a three-layer collapse mechanism [103, 224]. The formation of CNTs on the C face was presumed to be caused by the reaction of residual $O_2$ with SiC: $SiC + 1/2O_2 = SiO + C$ [103]. A CNT growth mechanism was proposed by Kusunoki's group. Over 1000°C, several graphite sheets are parallelly grown on the $(000\bar{1})$ SiC plane by the oxidation and evaporation of Si; At around 1300°C, $O_2$ penetrates underneath the graphite sheet and preferentially reacts with Si atoms to produce SiO gas. Driven by the SiO gas pressure, the graphite sheets are further deformed to form nanocaps. These carbon nanocaps are formed by the generation of bubbles of SiO gas on the SiC surface. The graphite sheets start to stand up on the $(000\bar{1})$ SiC plane. Finally, CNTs grow toward the interior of SiC [103]. Kusunoki also reported that when a layer of $Si_3N_4$ was deposited on the C face as a mask, the generation of graphite bubbles that were necessary for the formation of CNTs, was prevented during the temperature rising stage. Consequently, a continuous, epitaxial graphite layers grew on the C face [102].

Different from the Kusunoki's method, the graphitization system invented by our group can grow multilayer epitaxial graphene films on both faces of 4H- and 6H-SiC. No vertically aligned carbon nanotubes are found on either face. No significant morphology difference is found between regions covered by a $Si_3N_4$ mask and regions uncovered by a $Si_3N_4$ mask. The growth mechanism of epitaxial graphene on SiC in our growth system is not wholly understood. However, one thing is clear: the gas environment in this system plays a key role in the formation of high quality epitaxial graphene.

## *6.2 Experiment Equipment and Procedure*

### 6.2.1 Design of the Graphitization System

### 6.2.2 Graphitization Procedure

The graphitization furnace system and the graphitization procedure have been skipped for intellectual property reasons. A paper will be published when these issues have been resolved.

## *6.3 Result and Discussion*

A doped 6H-SiC wafer (No.2) with the Si face polished was the first one used for graphitization. Later, insulating 4H-SiC wafers (No.3-7) were extensively studied. 4H-SiC wafers are normally polished on both faces. Both the Si face and C face of a 4H-SiC sample are graphitized simultaneously. The graphitized SiC samples are characterized by AFM, SEM, TEM, STM, X-ray scattering, Raman spectroscopy, infrared Landau level spectroscopy, and transport experiments. The thickness, morphology, and quality of epitaxial graphene films on the surfaces of SiC depend on polytype, polarity, graphitization temperature, and time. The main results are summarized below.

1. Typical graphitization temperatures are above 1350°C from the thermocouple. (The real temperature on SiC samples may be 100-150°C higher than that from thermocouple reading.) The surfaces of a SiC substrate are modulated into irregular terraces by thermally-induced flow motion. Flat graphene films continuously grow over these SiC terraces. Gray or black color film can be seen on the surfaces after graphitization.

2. The surface morphology of SiC does not change unless the heating temperature is high enough (minimally 1300°C). SiC surfaces can be flattened by thermally induced surface flow motion at a temperature slightly below the graphitization temperature. No graphene film is identified on the thermally flattened SiC surface.

3. Both the Si face and the C face are heated simultaneously under the same graphitizaton conditions. But graphitization mechanism is different between the Si face and the C face of SiC.

a) Graphitization on the C face starts at a slightly lower temperature ( $< 50°C$) than on the Si face. The growth rate of a graphene film on the C face is much faster than on the Si face, and a thicker graphene film grows on the C face than on the Si face. The conductance of the graphene film on the C face is typically about one or two orders of magnitude higher than that on the Si face.

b) A graphene film starts to abruptly grow on the C face with a narrow temperature transition window ($\leq 20°C$) from SiC to graphene. The thickness of graphene films on the C face varies from few to dozens of graphene layers. Graphitization on the Si face undergoes a series of surface reconstructions before the first graphene layer forms. The thickness of graphene films on the Si face varies from one to about ten graphene layers.

c) A multilayer graphene film on the C face has several orientation rotations. Due to the relative rotations between graphene layers, the transport properties of graphene film on the C face resemble that of single graphene sheet. A multilayer graphene film on the Si face is a AB stacked, thin graphite film.

d) Epitaxial graphene films continuously grow over the SiC top surface. AFM images taken on graphitized SiC surfaces mainly reflect the morphologies of SiC top surfaces instead of graphene films. The surface morphologies on both the Si face and the C face of graphitized SiC substrates are sensitive to temperature, especially for very thin graphene films.

### 6.3.1 Graphitization of the Si Face of 6H-SiC

The No.2 wafer is a n-doped 6H-SiC with the Si face polished. The surface morphology of the Si face was observed by AFM before and after graphitization. The crystal structure of graphene film was characterized by LEED, and the thickness was estimated from the AES parameter fitting by Professor Philip First's group.

The surface morphology of SiC samples changes with the increasing temperature. For example, sample No.154 is graphitized several times at elevated temperatures (1200°C, 1300°C. 1400°C, and 1500°C) for 10 minutes as seen in Figure 6.1. After each heating, the

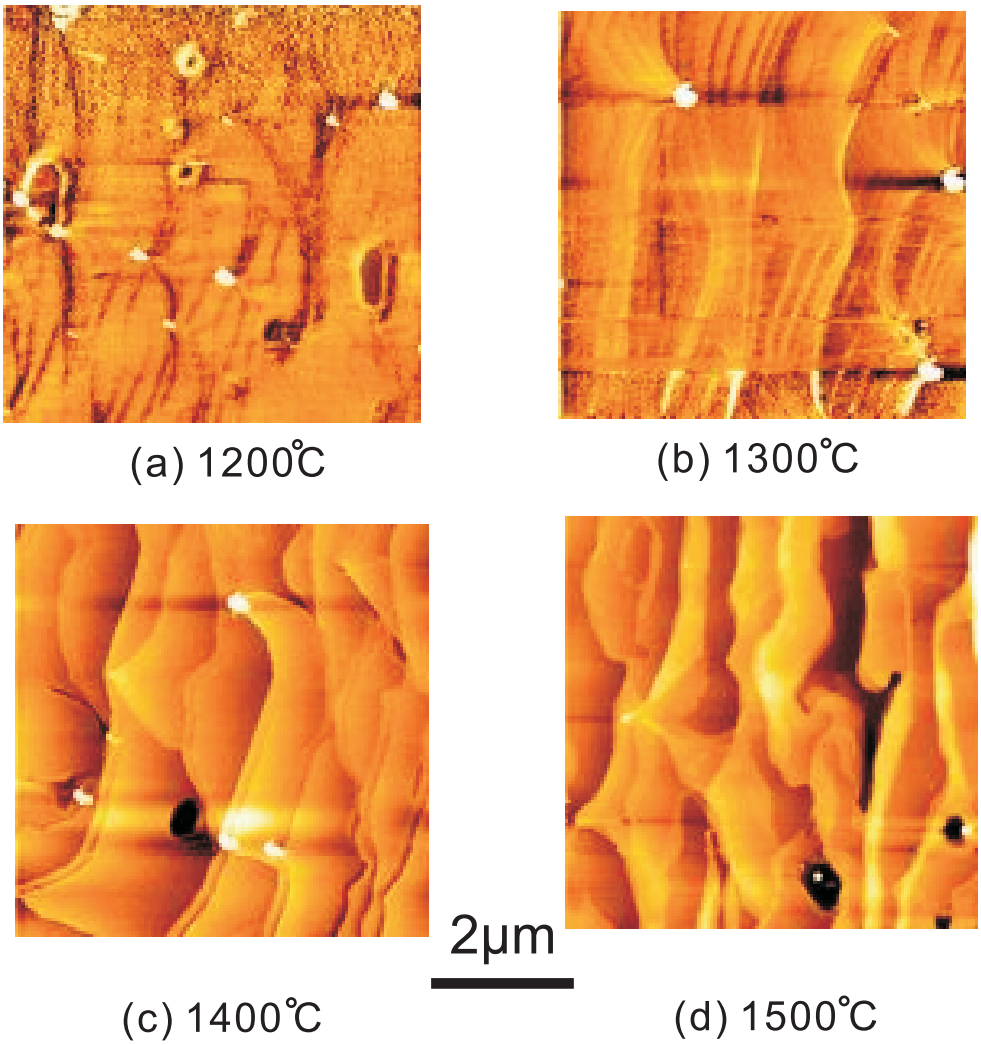


**Figure 6.1:** Surface morphology change with temperature on the Si face of a doped 6H-SiC wafer.

sample is removed from the furnace, scanned by AFM in air, then put back in the furnace for another higher heat treatment. Initially, the terraces on SiC are blurred. There are pinholes and particles on the surface. At higher temperatures (1300°C and 1400°C), these particles accumulate at corners of terraces and modify the orientation of terraces. At a even higher temperature (1500°C), some irregular stripe-like structures appear along the edges of terraces. The height profile change between adjacent terraces is abrupt with steep steps of 6-10 nm. Surfaces have more cracks and deep holes. On the whole, the tendency of terrace alignment is fairly well preserved even after a series of heat treatments.

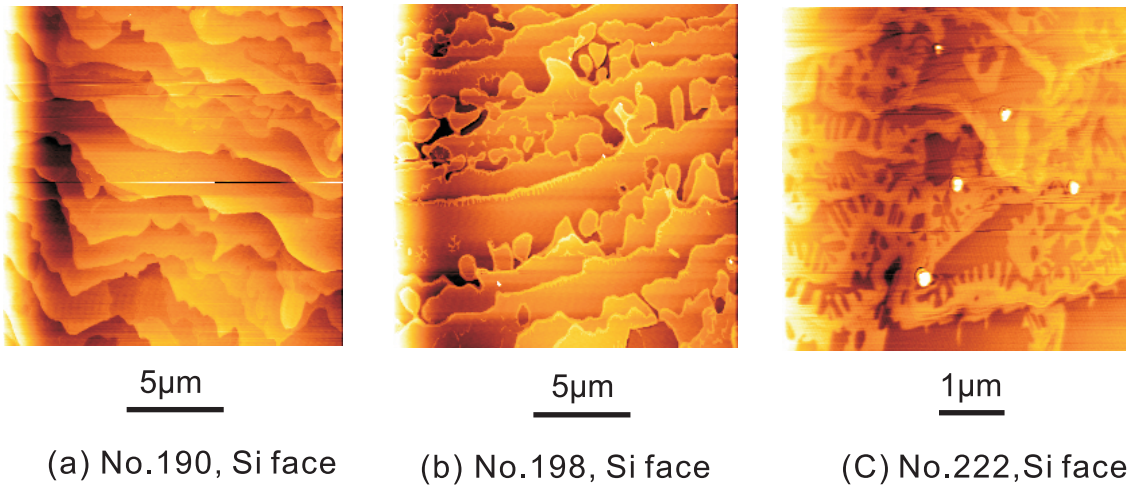


**Figure 6.2:** Surface morphology on the Si face of 4H-SiC (Wafer No.3). (a) A very thin graphene film on the sample No.190 (less than 2 layers estimated from the AES fitting). (b) A thin graphene film on the sample No.198. (c) A thick graphene film on the sample No.222.

### 6.3.2 Graphitization of the 4H-SiC

Later we focused on insulating 4H-SiC wafers. Graphene films grown on the Si face and on the C face of 4H-SiC show many distinctions in surface morphology, crystal structure, and transport properties.

#### *6.3.2.1 Surface Morphology of Graphene Films on the Si Face of 4H-SiC*

Like on the Si face of 6H-SiC, a graphene film on the Si face of 4H-SiC can more or less preserve the terraces of the hydrogen-etched SiC surfaces. This is more obvious for a very thin graphene film as shown in Figure 6.2(a). There are feature structures along the edges of terraces in Figure 6.2(a). These features are more easily identified on another sample (No.198) of similar thickness (see Figure 6.2 (b)). When more graphene layers grow on the surface, these kinds of feature structures appear not only along the edges but also on the terraces (see Figure 6.2(c)).

For the 4H-SiC No.6-7 wafers, Si face shows a different morphology from No.2-4 wafers. In Figure 6.3(a)-(b), regular terraces are aligned in the same orientation, and finger-like stripes are distributed on the terraces and are aligned perpendicular to the edges of terraces. The step heights between adjacent terraces are typically 1-4 nm as shown from Line scan

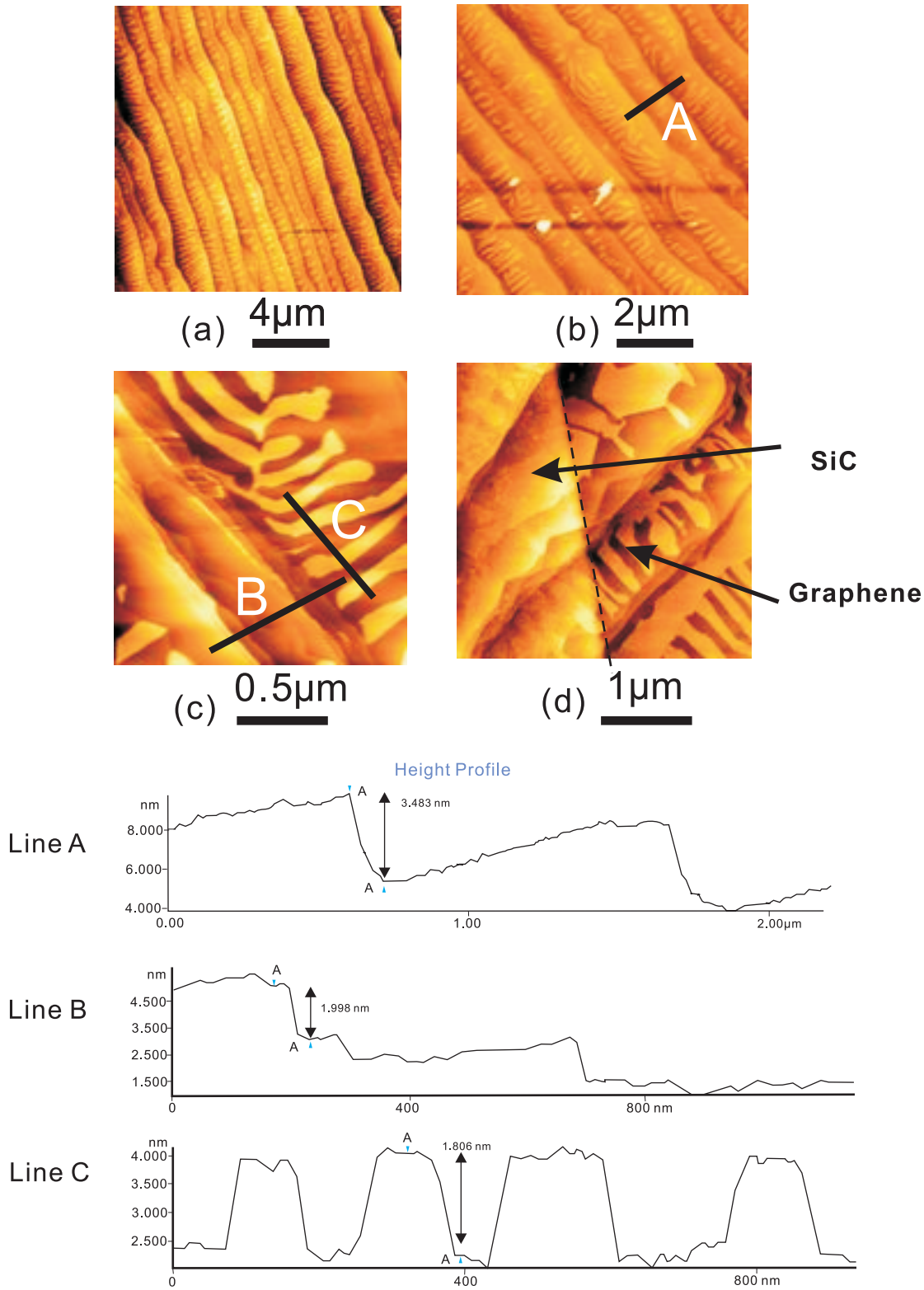


**Figure 6.3:** Surface morphology on the Si face of 4H-SiC (Wafer No.6). (a)-(c) AFM images on the graphitized Si face. (d) AFM image on patterned graphene after oxygen plasma etching. The left region is epitaxial graphene protected by an etch mask. The right region is the SiC surface after epitaxial graphene on top of it was etched away by oxygen plasma. Line scans A, B, and C exhibit the height profiles.

A and B. The heights of the finger stripes are within 2 nm as shown in Line scan C. In Figure 6.3(d), the right region is the epitaxial graphene film and the left region is the SiC surface after the top graphene film has been etched away by plasma oxygen. The terraces and finger stripes are continuous from the SiC region to the graphene region. That indicates that the surface AFM morphology really reflects the SiC surface instead of the graphene layers on top of the SiC. The graphene films continuously grow over these terraces and fine structures on the SiC.

#### *6.3.2.2 Surface Morphology of Graphene Films on the C face of 4H-SiC*

Without the hydrogen etching treatment, both faces of SiC can be flattened by thermal annealing in our furnace growth system. Figure 6.4(a)-(b) show the surface morphology on the C face of a 4H-SiC (wafer No.4) after being annealed at a temperature 20°C below the graphitization temperature for 10 mins. The top surface of this sample (No.444) is still electrically insulating. Neither graphene layers nor a carbon rich film are identified by LEED and AES (by Tianbo Li). That means that the flattened surface is achieved by the flowing of the SiC surface itself. The Flattened surface has regular terraces along the same orientation. AFM images taken on different locations on the same sample show terraces of different widths, which is most probably caused by tiny temperature inhomogeneities over the whole surface.

Figure 6.4(c) shows the surface morphology of another sample (No.415) that is still insulating after annealing. The shapes of terraces are modified by some small round particle-like bumps. Terraces are arched into these round particles. These round particles are not from external contaminants because they are observed only on the C face. The AES analysis on this sample does not detect any other elements except for Si, C, and O. These particles are possibly caused by the accumulation of excess Si atoms that could not evaporate immediately from the SiC substrate.

Very thin graphene films on the C face have nice terraces with pucker-like structures as seen in Figure 6.5(a). These pucker structures exist not only on the top graphene layer but also on lower graphene layers. The pucker structures are caused by the thermal contraction

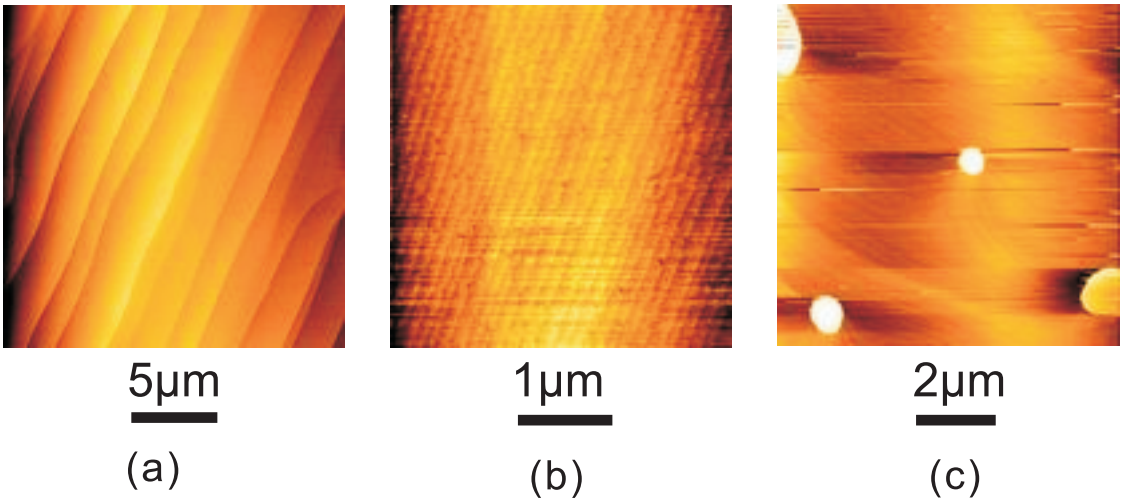


**Figure 6.4:** AFM images on the C face of ungraphitized 4H-SiC samples (wafer No.4). (a)-(b) Regular terraces observed on different locations on the sample No.444. (c) Terraces are modulated by round particles on the sample No.415.

between SiC and graphene layers due to their thermal expansion coefficient mismatch and the sharp steps between SiC terraces. Similar surface morphologies were found after top layers were gently oxidized away by water vapor ($10^{-5}$ Torr) in UHV for seconds (with the aid of Kristin Shepperd in the group of Professor Thomas Orlando) or mechanically peeled by Scotch tape, rubber cement, or polydimethylsiloxane (PDMS). These pucker structures disappear when graphene layers are completely etched away by oxygen plasma.

For typical graphene films ($\sim$ 10 layers) on the C face, nice, regular terraces are not observed under AFM. Figure 6.5(b) shows flat domains of several $\mu m^2$. Cracks, holes, and pucker structures are seen near boundaries or apexes between flat domains. These defects are attributed to complicated surface modification of SiC during graphitization (such as the diffusion of Si atoms from the deep substrate to the graphene film surface) and complex reconstructions at the interface between the SiC and the graphene film.

The surface morphology of SiC surface can be seen clearly in Figure 6.5(c). After oxygen plasma etching, unprotected graphene films are etched away and bare SiC surfaces are scanned under the AFM. Terraces on the SiC regions are continuous with those on the graphene regions that are protected from etching by an etch mask (PMMA). It is clear that the AFM images mainly reflect the surface morphology of the SiC surface rather than the

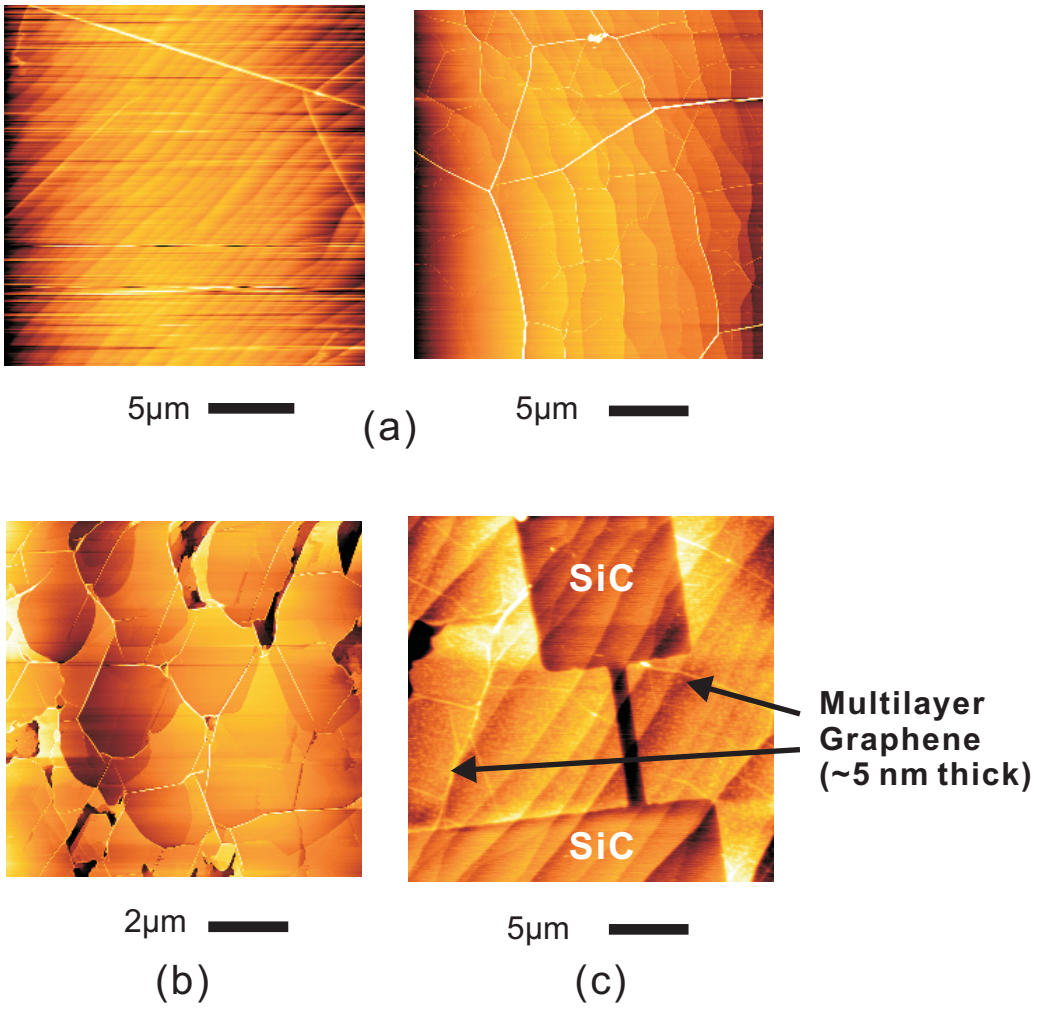


**Figure 6.5:** AFM images on graphene films grown on the C face of 4H-SiC. (a) A very thin graphene film. (b) A typical thick graphene film ($\geq$ 10 layers). (c) A patterned graphene structure after oxygen plasma etching

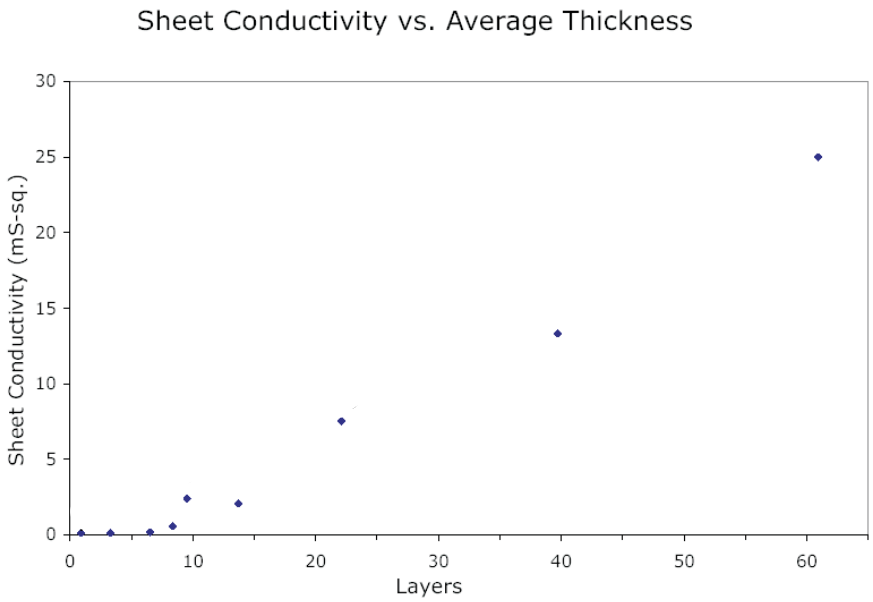


**Figure 6.6:** Plot of the sheet conductivity of graphene films versus the number of layers determined by the Woollam ellipsometer.

graphene film itself.

### 6.3.3 Thickness Measurement of Epitaxial Graphene

For a thin graphene film (less than 4-5 layers), the number of layers can be estimated by the ratio of C/Si peaks measured in the AES. For a thicker graphene film, we use other methods. AFM is a very efficient method to measure the thickness of the graphene film since AFM is sensitive to height change. AFM on patterned graphene structures gives us very accurate results as seen in Figure 6.5 (c). However, AFM can only measure locally the thickness and its accuracy is strongly affected by the surface quality of the SiC substrate. Ellipsometry is another reliable method to determine the film thickness and optical properties. Data are obtained through measuring the change in polarization state of the incident light when the light is reflected off the surface of (or transmitted through) a sample. The Woollam ellipsometer in MiRC does not provide a standard model to measure the graphene film thickness on a SiC substrate. Michael Sprinkle in our lab developed a model to measure the average graphene film thickness on a scale of hundreds of $\mu m^2$. In this model, properties of bulk graphite are chosen as an approximation for graphene. For a thin graphene film, the

film thickness determined by the Woollam ellipsometer is very close to what is estimated from the AES analysis. We have extended the Woollam ellipsometer method to measure thicker graphene films (several to tens of layers). Besides this method, the sheet resistance of the graphene film can also indicate qualitatively how thick the graphene film is. Figure 6.6 plots out the sheet conductivity of the graphene film versus the number of layers measured by the Woollam ellipsometer.

### 6.3.4 Comparison of Epitaxial Graphene Between the C face and the Si face of 4H-SiC

The epitaxial graphene films grown in our system are characterized by LEED, AES, and X-ray reflectivity, etc. Graphene films grown on the Si face and the C face possess different structural properties that are discussed below.

Sample No.164 (wafer No.3) was graphitized at 1400°C for 10 minutes. AFM images were taken on both faces after graphitization as seen in Figure 6.7(a)-(b). The Si face has terrace-like structures of $\sim \mu m$ wide and 1-4 nm high. The C face has flat domains of several to tens of $\mu m^2$. Later this sample was characterized by AES and LEED in UHV chamber by Tianbo Li in the lab of Professor Phillip First.

Figure 6.7(c)-(d) shows AES taken on both faces of this sample. Only Si, C, and O absorption peaks are identified. The relation of the C/Si peak ratio and the number of layers was described in the thesis of Tianbo Li [109]. The C/Si peak ratio on the Si face is about 3.8, corresponding to 1-2 graphene layers. The C/Si peak ratio on the C face is about 13.3, corresponding to 3-4 graphene layers.

LEED patterns were also taken on both faces at different excitation energies. Figure 6.7(e) is taken on the Si face. Sharp diffraction spots from the SiC substrate are clearly seen with a six-folding symmetry of the SiC crystal structure. Sharp diffraction spots from top graphene films are also observed with a 30 degrees rotation relative to the spots from bulk SiC. The satellite spots around the bulk SiC spots are due to multiple-scattering. Figure 6.7(f) is taken on the C face. Diffraction spots from both the SiC substrate and the graphene film are seen in the LEED when the graphene film is very thin. But the graphene spots on the C face are blurred, and slightly stretched around the LEED center.

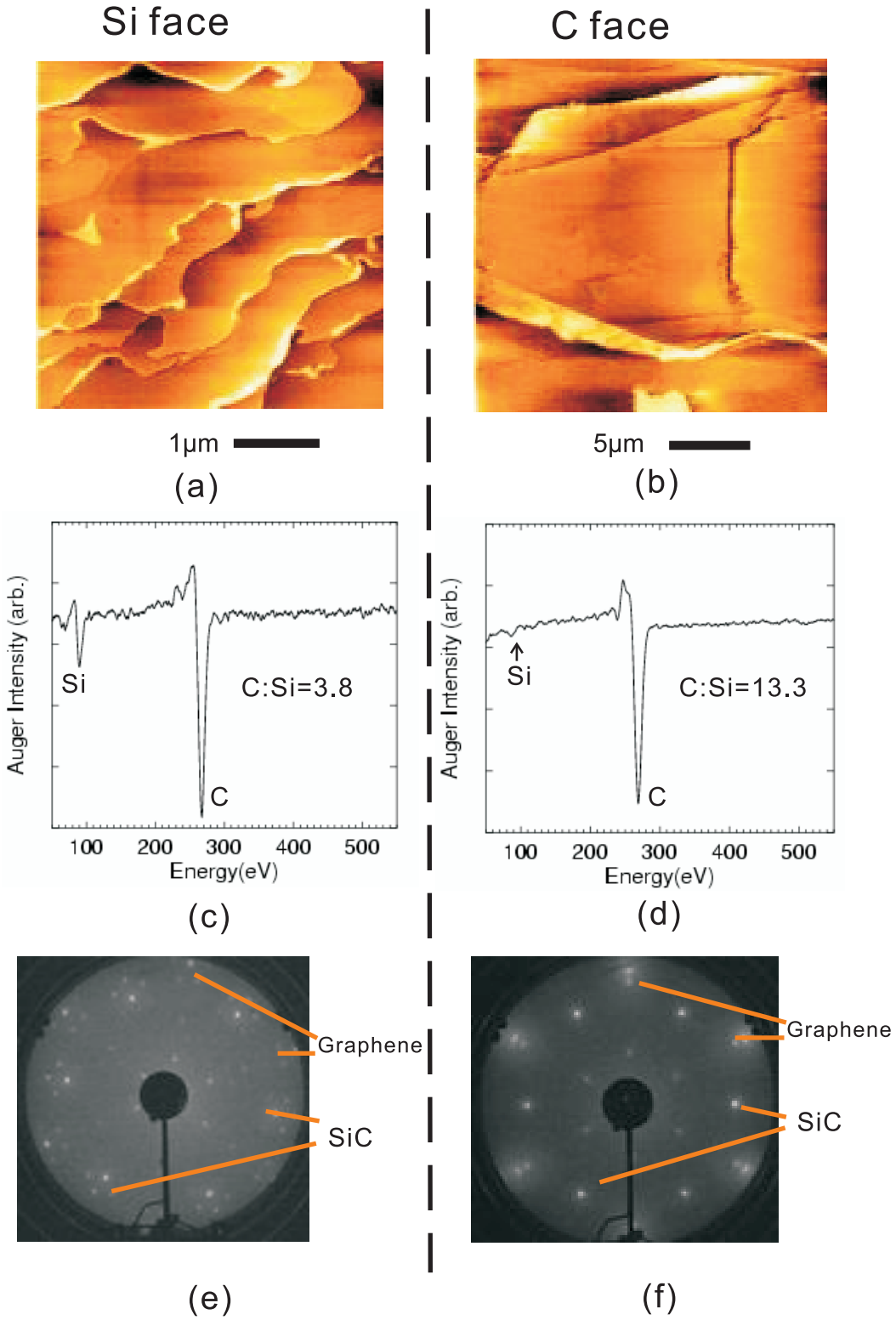


**Figure 6.7:** Comparison of graphene films grown on the Si face and on the C face of the sample No.164 (4H-SiC). (a) AFM on the Si face. (b) AFM on the C face. (c) AES on the Si face. (d) AES on the C face. (e) LEED on the Si face (Electron energy = 61.8 eV). (f) LEED on the C face (Electron energy = 71.2 eV).

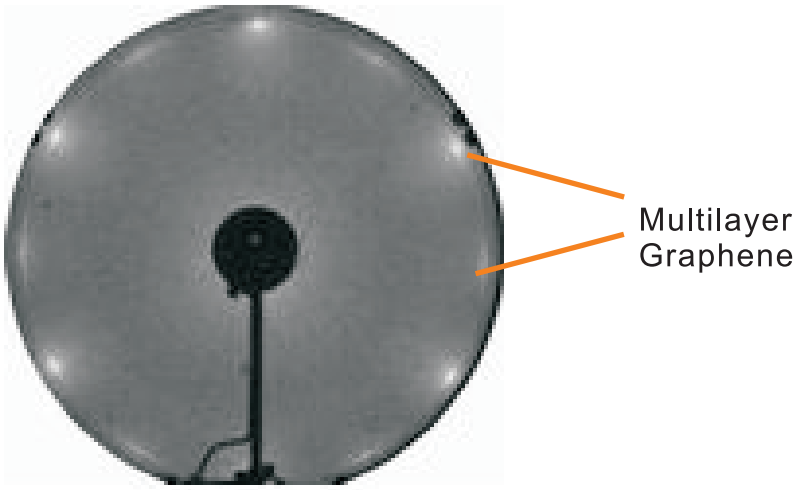


**Figure 6.8:** LEED on a thick graphene film on the C face of the sample No.206 (4H-SiC). Electron energy=69 eV. Only graphene diffraction spots are seen.

These blurred diffraction spots indicate the graphene film is not well oriented on the surface. They are caused by several relative rotations between different graphene layers in addition to a rotation between the graphene film and the SiC substrate [75, 76, 225].

For a thicker graphene film (more than 4 layers) on the C face, no Si is detected within the limit of the AES resolution. Only sharp diffraction patterns of the thick graphene film are seen in the LEED for moderate excitation energies. In Figure 6.8, individual diffraction spots from a thick graphene film (more than 4 layers) tend to merge into a full ring. The brighter spots on the ring indicate that the multilayer graphene film on the C face is not randomly oriented and graphene layers have specific preferential orientations. X-ray scattering experiments done by Professor Edward Conrad and graduate student Johanna Hass provide more information about the physical and crystal qualities of graphene films [75, 76].

### 6.3.5 STM on Epitaxial Graphene

STM images of our epitaxial graphene samples were taken on the C face of 4H-SiC by students in the lab of Professor Phillip First. Figure 6.9(a)-(b) shows images taken on sample No.205 and No.206 (from wafer No.3). On the surface, there are atomic flat graphene regions that are accompanied by some amorphous carbon structures (Left: about 1 nm high)

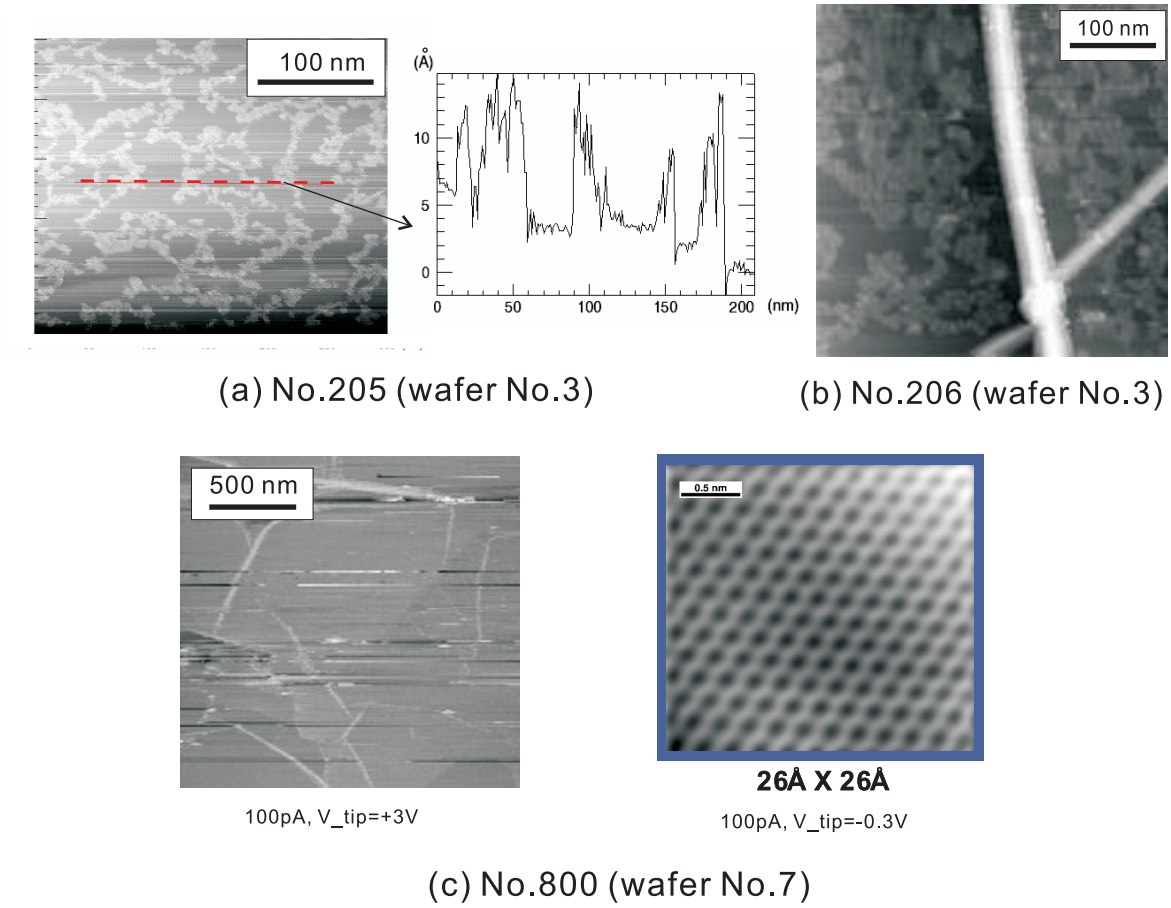


**Figure 6.9:** STM images on the graphitized C face of 4H-SiC samples. (a) No.205 (wafer No.3) (b) No.206 ( Wafer No.3). (c) No.800 (Wafer No.7).

and pucker like structures (Right: about several nm high) [109]. Figure 6.9(c) shows STM images taken on the most recent sample No.800 (from wafer No.7). On this sample (No.800), amorphous carbon structures are not observed. A high resolution STM image taken on a flat region clearly shows the atomically resolved, honeycomb pattern of graphene. The origin of the amorphous carbon is still under investigation.

### 6.3.6 Cross-section View of Graphene by HRTEM

A 4H-SiC sample No.447 (wafer No.4) was graphitized and shipped to D. Ugarte at LNLS, Brazil for the high resolution transmission electron microscope (HRTEM) imaging. For a HRTEM specimen, this sample was cut into half. The faces were glued together, and thinned by polishing, and then ion milled.

As seen in Figure 6.10(a), the crystal lattices of 4H-SiC are clearly displayed on the left

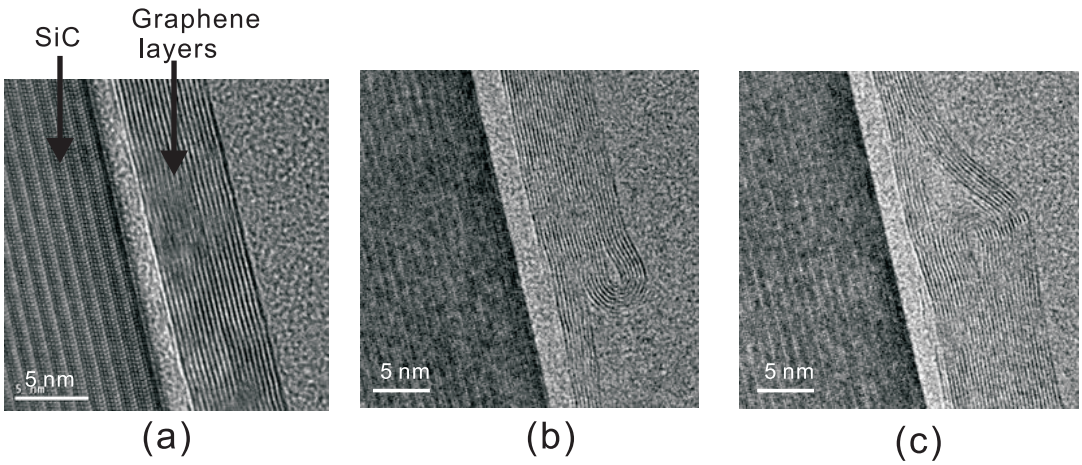


**Figure 6.10:** The cross-section view of the graphene-SiC system by HRTEM .

region. On the right region, the graphene layers are parallel to each other and well aligned with the crystal lattice of the 4H-SiC substrate. Since the graphene film is very fragile to mechanical handling during the specimen preparation, the graphene layers are peeled from the SiC substrate, which explains the separation at the interface region. The unusual folded stacking of graphene layers (Figure 6.10 (b)-(c)) is also caused by the HRTEM sample preparation.

### 6.3.7 X-ray Reflectivity Experiment on Epitaxial Graphene

The X-ray reflectivity experiments and data analysis were done by the group of Professor Edward Conrad. The main goal is to study the crystal structure quality of epitaxial graphene on both faces of SiC, especially on the C face of 4H-SiC. Their main conclusions are summarized below [75, 76].

- Graphene films on both the Si and the C Face of SiC are extremely smooth (rms corrugation less than 0.05 Åon the C face and less than 0.5 Åon the Si face).
- For graphene on the C face, the structural domain sizes are much larger than those on the Si face.
- The first graphene layer at the interface is in fact an insulating 'buffer' layer tightly bound with the last SiC layer .

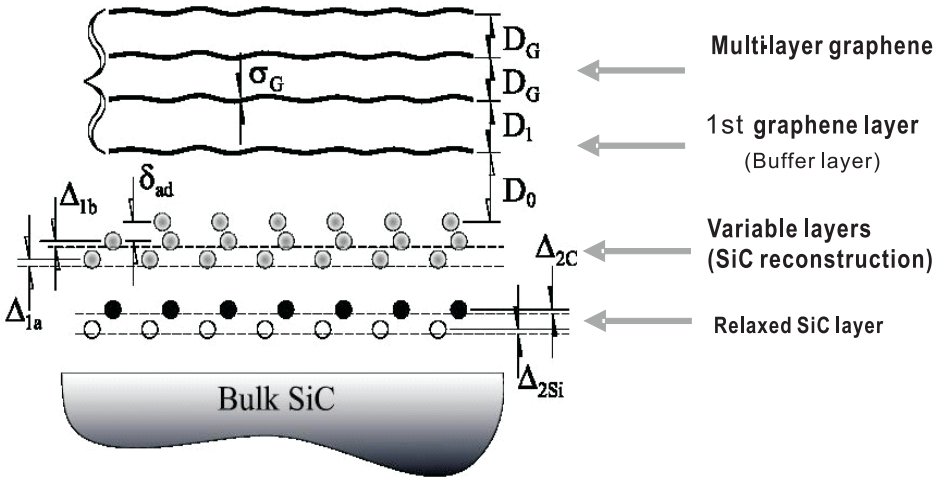


**Figure 6.11:** Schematic representation of epitaxial graphene on the C face of 4H-SiC.

- The multilayer graphene film on the C face is not Bernal stacked.

From best fits to the X-ray reflectivity data, a schematic model of the epitaxial graphene on the C face of 4H-SiC has been proposed [76]. That model explains why the multilayer epitaxial graphene film is distinct from the bulk graphite [76, 225]. As shown in Figure 6.11, there are two types of reconstructed layers between the bulk SiC and the first graphene layer. The first graphene layer is strongly $sp^3$ bonded with the substrate rather than by the weak van der Waal's interaction that is characteristic for the bonding between graphene layers. From the *ab initio* calculations, this first graphene layer is insulating and acts as a buffer layer between other graphene layers and the substrate [225]. The graphene layers above the buffer layer are very flat and have very weak interactions with the bulk substrate. The relative rotations between graphene layers induce stacking faults that break the AB stacking sequence in Bernal graphite. As a result, multilayer epitaxial graphene films on the C face of SiC electronically resemble a single graphene sheet, as has been confirmed by transport measurements and micro-Raman scattering experiments [19, 40, 48, 237]

## *6.4 Summary*

A homemade induction furnace growth system was designed for epitaxial graphene growth in vacuum. High-quality multilayer graphene films are grown epitaxially on the Si face and C face of 4H- and 6H-SiC substrates by thermal decomposition of SiC at high temperatures.

The crystal structure of graphene films have been characterized by AFM, LEED, AES, STM, HRTEM, and X-ray reflectivity. Significant distinctions exist on epitaxial graphene grown on the Si face and the C face with respect to thickness, surface morphology, and crystal structure. A graphene-SiC interface model on the C face is proposed from the X-ray reflectivity experiments and other evidences.

# CHAPTER VII

# FABRICATION OF EPITAXIAL GRAPHENE DEVICES

Epitaxial graphene can be patterned into various structures by standard lithography and semiconductor processing techniques. A typical device fabrication process includes photolithography or E-beam lithography, metal deposition, plasma etching, plasma dielectric deposition, wirebonding, and others. This chapter will introduce briefly relevant processing techniques used in the epitaxial graphene device fabrication, and then describe the whole processes to produce graphene side gated field effect transistors (FETs) and top gated FETs. Other graphene devices are given as examples to demonstrate the potential and flexibility of epitaxial graphene for semiconductor processing.

## *7.1 Lithography*

### 7.1.1 Photolithography

Lithography is the cornerstone of modern IC manufacturing. Photolithography is the dominant lithographic technique for the industrial wafer processing because of its high throughout, repeatability, and flexibility.

Photolithography transfers geometric shapes on a photomask to the surface of a wafer by the exposure of photoresist to a light source at a certain wavelength. In a typical photolithography process, a photoresist is spun onto a wafer to form a uniform thin layer on the surface. A photomask is placed between a light source and the resist layer. The resist layer is selectively exposed to the light at a certain wavelength (in the range of UV, DUV, or EUV). After the resist development, the patterns on the photomask are transferred to the resist layer.

There are two kinds of photo resists: positive and negative. For a positive resist, the resist on the exposed regions changes its chemical structure so that it becomes more soluble in a developer (selective wet solvent). The developer can easily remove the resist on the exposed regions. A negative resist behaves in an opposite manner. The negative resist

on exposed regions is polymerized and become difficult to dissolve in a developer. The developer only removes resist on the unexposed regions. Nowadays, positive resists are dominant in IC manufacturing because of their better controllability for feature structures.

A typical photolithography process with positive resists are listed below. The scheme is shown in Figure 7.1(a). The purpose of each step are explained briefly. Some steps can be skipped for specific applications.

1. Wafer cleaning. (to remove particles on the surface as well as any organic, ionic, and metallic impurities)
2. Dehydration baking. (to remove any moisture on the surface)
3. Primer coating. (to coat the wafer with a primer (such as HDMS) to improve the adhesion and uniformity of the following photoresist coating )
4. Photoresist coating. (to coat the surface with an uniform photoresist layer)
5. Soft baking. (to remove the solvents from the resist layer)
6. Mask alignment. (to align the patterns on the mask with the wafer surface)
7. Exposure. (to expose the resist to an UV or DUV light; three primary exposure modes: contact printing, proximity printing, and project printing)
8. Development. (to remove the unwanted resist on the surface by a developer)
9. Hard baking. (to harden the photoresist and to improve the adhesion of the photoresist to the wafer surface)

Other processes can be executed after the photolithography step, including metal liftoff deposition, wet/dry etching, and ion implantation with the resist as a mask.

The minimal geometry (feature size or critical dimension (CD)) of patterns on the resist is dependent on resist type, thickness, the wavelength of the UV light, the feature size of the photomask, and development. The feature size achieved by a typical photolithography system is about 65-90 nm in industry. For the most advanced commercial photolithography

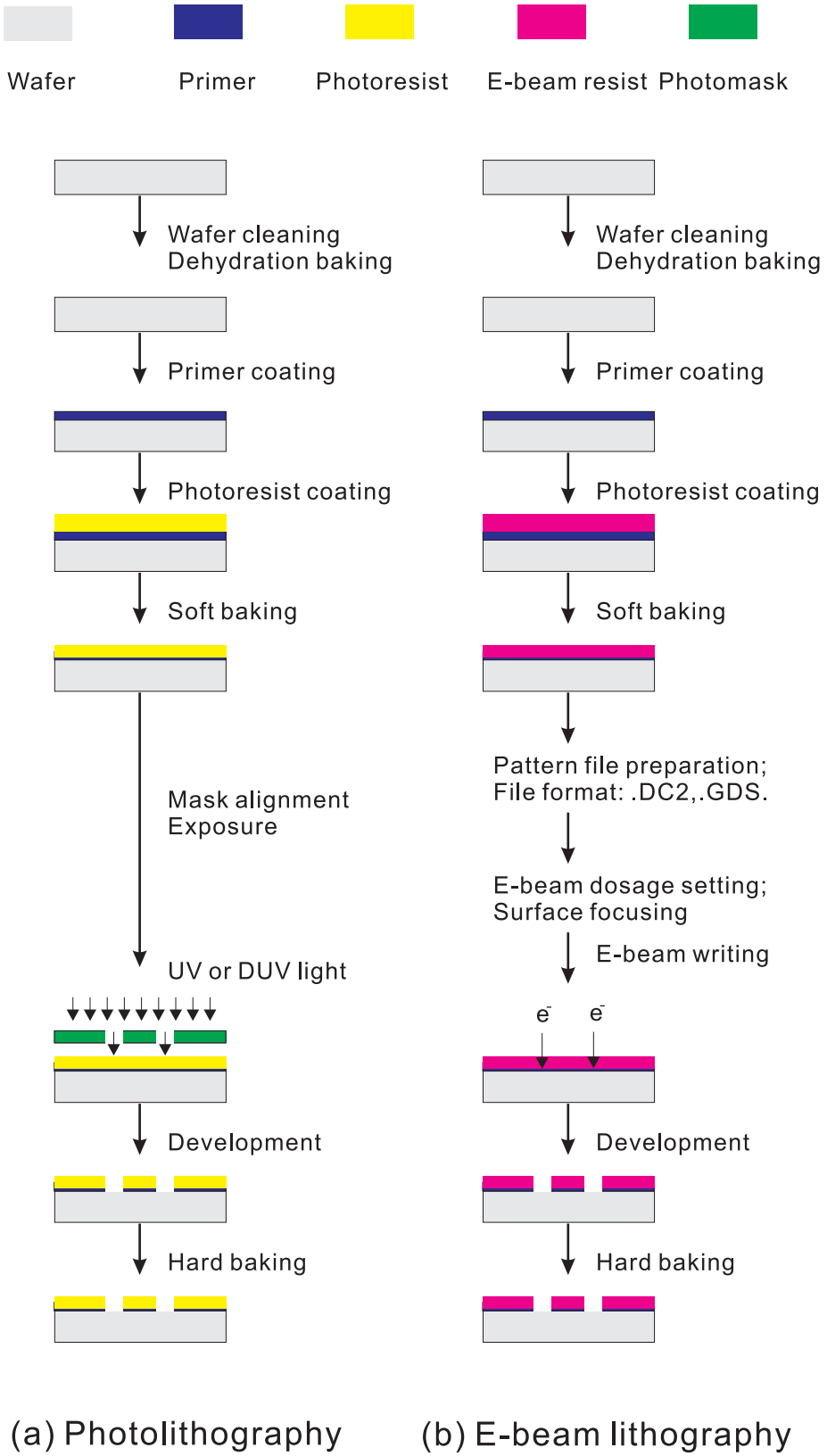


**Figure 7.1:** Scheme of the photolithography process and the E-beam lithography process with positive resists. (a) Photolithography. (b) E-beam lithography.

systems, the feature size of 45 nm can be achieved with the new development in immersion lithography, DUV light source, new photoresist, and other new technologies. A 500 nm feature size can be achieved in the photolithography Fab in the cleanroom of MiRC at the Georgia Institute of Technology.

The main limitation of photolithography is the cost of masks, especially those with very small feature patterns. Masks have to be replaced after a certain period due to contaminants and abrasion.

### 7.1.2 E-beam Lithography

E-beam lithography can fabricate devices with feature sizes down to 10 nm. E-beam lithography does not require a photomask, and an electron beam is used to draw patterns directly on a resist. The wavelength of electron (for example, about 0.2-0.5 Å at 100 keV) is much shorter than the those of DUV light sources (365 nm and 405 nm in MiRC). The electron beam can pattern very fine structures down to less than 10 nm. Therefore, E-beam lithography is widely used in photomask-making, low-volume production of semiconductor components, and research development. E-beam lithography shows its particular advantage in quantum transport research in nano-scale (several to tens of nm) devices. But E-beam lithography is not suitable for high-volume manufacturing because the electron beam has to scan serially across the wafer surface, which is time consuming.

Routinely, the size of an electron beam can be reduced to a few nm. However, the practical, achievable resolution on a sample is limited mainly by electron optic aberrations, and scattering of electrons in resists and on substrate surfaces. Forward scattering and back scattering are the two main scattering mechanisms that occur during the E-beam writing.

In forward scattering, an incident electron inelastically collides with the electrons of target atoms. The electron not only changes its direction with a small angle deviation from the incident direction, but also transfers part of its energy to the atoms that become excited (one of its electrons goes into an excited level) or ionized (one of its electrons leaves the atom, creating a secondary electron that travels in the material). The forward scattering broadens the size of electron beam and widens the patterns on the resist.

In back scattering, the incident electron elastically collides with the nucleus of the atoms, and retains its energy but changes its direction at a large angle after each collision. After several large angle back scatterings, the electron is possibly bounced back through the resist, far away from the regions of the incident electron beam. Therefore, back scattering causes additional resist exposure.

These above scattering effects (also called the proximity effect) cause unintentional exposure on areas surrounding the to-be-patterned regions by the incident electron beam. Sometimes,written patterns suffer significant variations from the original design because of the proximity effect. Higher energy electrons or thinner photoresist layer can suppress the forward scattering. The back scattering is determined mainly by the atomic mass of resist molecules and the substrate. To reduce these additional exposures by scattering, the pattern has to be slightly modified in shape to counteract the proximity effect.

There are two kinds of E-beam resists: positive and negative. Positive resists on the exposured regions by electron beam are dissolved in a developer. Negative resists on the unexposured regions are dissolved in a developer. Below, I introduces several E-beam resists supplied in MiRC: polymethylmethacrylate (PMMA), ZEP-520A, and hydrogen silsesquioxane (HSQ). PMMA is an ultra-high resolution, high current positive resist used for nanolithography. It sticks well to almost any surface and gives reproducible pattern results. But PMMA has poor sensitivity and poor dry etch resistance. Standard PMMA products include 495k and 950k molecular weights (MW) in a wide range of film thicknesses formulated in chlorobenzene or the safer solvent anisole. MiRC provides 2%, 4%, 7%, and 11% 950k PMMA in anisole. ZEP-520A is also a very high resolution positive resist like PMMA. ZEP-520A is simple to use and gives reproducible results. Compared to PMMA, ZEP-520A has an advantage of lower E-beam exposure dosage and good dry etch resistance. ZEP-520A's disadvantages are poor adhesion (HMDS is used as the adhesion layer) and undercut profiles. HSQ was developed originally as a low k dielectric in microelectronics fabrication. Later HSQ is used for high resolution, negative-tone features patterning by E-beam.

A typical process for E-beam lithography with a positive resist for epitaxial graphene device fabrication is list below. The scheme is shown in Figure 7.1(b).

1. Wafer cleaning. (to remove particles on the surface as well as any organic, ionic , metallic impurities)
2. Dehydration Baking. (to remove any moisture on the surface)
3. Primer coating. (to coat the wafer with a primer (such as HDMS) to improve the adhesion and uniformity of the following photoresist coating)
4. E-beam resist coating. (to coat the surface with a uniform resist layer)
5. Soft baking. (to remove the solvents from the resist layer)
6. Pattern file preparation. (to design the patterns with CAD software; executable file formats include .GDS and .DC2)
7. E-beam dosage setting. (to achieve the expected e-beam exposure dosage for different patterns)
8. Surface focusing. (to ensure the electron beam spot exactly converges on the resist surface)
9. E-beam writing. (to pattern the resist by blanking or not blanking the electron beam)
10. Development. (to dissolve the unwanted resist with a developer)
11. Hard baking. (to harden the resist and improve the adhesion of the resist to the wafer surface)

The E-beam facilities (used in our epitaxial graphene device fabrication) include the JSM 5910 system in the School of Physics and the JEOL JBX 9300 system in MiRC at Georgia Institute of Technology. The JSM 5910 typically operates in an electron beam current range of 10 pA -9 nA at an acceleration voltage of 5-30 kV. Smaller beam current and higher acceleration voltage are chosen to pattern the fine structures for a better resolution. The highest patterning resolution achieved on the JSM 5910 system is about 60 nm. The JEOL JBX 9300 system can pattern much finer structures than the JSM 5910 system. 6 nm PMMA ribbons can be patterned on a Si substrate. 10 nm PMMA ribbons and 10-15

nm HSQ ribbons have been achieved on epitaxial graphene films. In this thesis work, these two systems are combined together to fabricate graphene devices.

## *7.2 Semiconductor Processing Techniques: Deposition and Etching*

### 7.2.1 Film Deposition

Film deposition techniques can be categorized into different subsets. Based on the materials, the deposition could be metal deposition or dielectric (low-k, high-k) deposition. Based on the deposition method, the deposition could be physical vapor deposition (PVD), chemical vapor deposition (CVD), or electrochemical deposition. PVD and CVD are used widely to deposit metal and dielectric materials in IC manufacturing.

#### *7.2.1.1 PVD Deposition*

PVD is a thin-film deposition process in which a material (metal, alloy, compound, or composite) is either evaporated or sputtered onto a substrate surface in vacuum. Chemical composition of the deposited material is not altered in the process. PVD can be used to deposit most metals and some dielectric materials. Dielectric films after PVD deposition generally have poor insulating capability because of holes and defects in the films.

There are three typical methods for PVD: E-beam evaporation, thermal evaporation, and sputtering deposition. An E-beam evaporator is used normally to coat samples with various metals. A thermal evaporator is chosen when materials (like photoresists and E-beam resists) on the substrate are sensitive to x-ray radiation from E-beam. These two methods deposit materials only on the surface that is facing the evaporated material source and are good for metal liftoff deposition. Sputtering deposition has a very good step coverage over uneven structures and is good for trench filling. A DC sputterer is used for metal deposition, and a RF sputterer is used for dielectric material deposition.

In the cleanroom of MiRC, the CVC E-beam evaporator is used to deposit Pd/Au, Al, Ti/Au, Cr/Au, or Pd-Ni contact pads. The PVD75 filament evaporator sometimes is used to deposit metal contacts when photo resist or E-beam resist coats the sample surface. The CVC DC Sputterer and the CVC RF Sputterer in MIRC are barely used in the process of graphene device fabrication.

#### *7.2.1.2 CVD Deposition*

CVD is a chemical process to grow thin films on substrates. In a typical CVD process, one or more volatile precursors flow into the reaction chamber, react and/or decompose near the substrate surface to form a thin film. Volatile byproducts are removed out of the reaction chamber. CVD can happen under atmosphere pressure (APCVD), low pressure (LPCVD), and ultrahigh vacuum (UHVCVD). CVD deposition happens at lower temperatures, which is often critical in the manufacture of semiconductors. Usually, CVD is used to deposit materials in various forms, including monocrystalline, polycrystalline, amorphous, and epitaxial. CVD is commonly used to deposit Si, $SiO_2$, $Si_xN_x$, TiN, W and other low-k, high-k dielectric materials.

Among various CVD methods, plasma-enhanced CVD (PECVD) utilizes plasma to enhance chemical reaction rates of the precursors. In the MiRC cleanroom, Unaxis PECVD and Plasma-Therm PECVD are used to deposit materials such as $SiO_2$, $Si_xN_y$, and SiC polycrystal. Typically, the insulating characteristics of $SiO_2$ and $Si_xN_y$ film deposited in these two CVD systems are not good unless the films are thick enough ($\sim 1\mu m$). A $SiO_2/Si_xN_y$ multilayer film is claimed to give a better insulation.

### 7.2.2 Etching

Film etching is used to selectively remove some materials or structures from the surfaces of substrates. Etching is categorized into different subsets: wet etching or plasma etching; physical etching or chemical etching; and conductor etching or dielectric etching.

There are two key factors in etching: etch selectivity and etch directionality. Etch selectivity is the ratio of the etch rates of the different materials in an etch process. For a desired etch process, the etch rates on the mask and the underlying substrate are almost zero, while the etch rate on the to-be-etched substrate is very significant. Chemical etching is very selective because etch rates on different materials are strongly dependent on the chemical reaction effects. On the contrary, physical etching such as sputtering is much less selective to different materials. Etch directionality is a measure of the relative etch rates in different directions, usually vertical direction versus lateral direction. Isotropic etching

occurs when the etch rates are the same in all directions. Anisotropy etching typically occurs when the etch rate in one direction (such as vertical) is much faster than in another direction (such as lateral). Industry widely uses anisotropy etching because it can transfer the well-designed patterns from etch masks onto the underlying film. On the whole, physical etching is more anisotropic but less selective, while chemical etching is less anisotropic but more selective.

Wet etching is a chemical etching process in which the material is isotropically etched away by chemical reactions in an etchant solution. Wet etching can be used to etch away oxide, metals, and other materials. Plasma etching (or dry etching) can be used to etch thin metal films and dielectric materials. Compared with wet etching, plasma etching is the main stream in industry etching because of several reasons. First, plasma has very reactive species that can etch more vigorously than in a nonplasma environment. Second, plasmas etching happens in a clean environment with fewer contaminants. Third, both chemical etching (reactive chemical components) and physical etching (ionic components) coexist in plasma etching. Therefore, high selectivity and high anisotropy are achieved in plasma etching systems.

In the cleanroom of MiRC, the most operated plasma dry etchers are Plasma-Therm RIE (reactive ion etcher) and Plasma-Therm ICP (inductively coupled plasma). For graphene device fabrication, the RIE etcher is used to etch photo resists, E-beam resists, $SiO_2$, $Si_xN_y$, carbon film, and thin metal films. The ICP etcher is used to etch devices with sub 100 nm features when high directionality is required. The ICP etcher has much better anisotropy because it has two power RF suppliers that are used separately to generate dense plasma gases and to accelerate them to the target. For a higher anisotropic etching on the fine structures ($\leq$ 100 nm) of graphene devices, great efforts have been made to design etching masks and to optimize etching parameters.

## *7.3 Fabrication of Field Effect Transistors (FETs)*

### 7.3.1 Top Gated FETs

A high-quality, insulating layer is the key factor to successfully fabricate top gated graphene FETs. We have tried CVD-grown $SiO_2$ and $Si_xN_y$ films that have the problem of gate leakage. $Al_2O_3$ and $HfO_2$ films have been deposited on our samples by our collaborators, and both films give good insulation. Deposition of these two materials requires delicate operation and good equipment. For our FETs project, I choose the HSQ as the dielectric material.

The procedure to produce top gated graphene FETs is listed below. It includes three E-beam patternings, two metal depositions, three resist spin coatings, three resist developments, and one dry etching.

1. Plane epitaxial graphene growth on a 3.5 mm × 4.5 mm 4H-SiC piece.
2. Deposition of metal contact Pd/Au (5 nm/100 nm) by an E-beam evaporator. (Base pressure: $2 \times 10^{-6}$ torr; evaporation rate: Pd (1.0 Å per second), Au (1.0-1.5Å per second))
3. PMMA spin coating and baking. (7 % PMMA, spin speed: 5k RPM; baking: 180 °C for 60 seconds)
4. 1st E-beam patterning on PMMA to define graphene ribbons.
5. PMMA development. (Developer: MIBK/IPA=1/3; developing time: 30 seconds)
6. RIE pure oxygen etching. (Power: 100 W; pressure: 100 mtorr; flow rate: 20 sccm; etching time: 60 seconds)
7. PMMA removal with acetone. (30 minutes)
8. HSQ spin coating and baking. (HSQ(XR-1541 6 %):MIBK = 2:1, spin speed: 10 k RPM; baking: 250°C for 90 seconds)
9. 2nd E-beam patterning on HSQ to define the HSQ insulating layer over the graphene ribbons.

10. HSQ development (Developer: AZ300MIF; developing time: 60 seconds)

11. MMA/PMMA bilayer spin coating and baking. (Bottom layer: MMA, spin speed 5 k RPM, baking: 150°C for 60 seconds; Top layer: PMMA (3%), spin speed: 5 k RPM, baking: 180°C for 60 seconds)

12. 3rd E-beam patterning on MMA/PMMA bilayer to define the regions for top gate electrodes.

13. Deposition of top gate electrodes (60 nm Al) by an E-beam evaporator. (Base pressure: $2\times10^{-6}$ torr; evaporation rate: 1 Å per second)

14. Liftoff of MMA/PMMA bilayer by acetone. (30 minutes)

15. Wire bonding and preliminary electrical test.

An epitaxial graphene sample is coated with PMMA and patterned into different ribbon structures by E-beam lithography. Then the sample is dry-etched by a pure oxygen plasma in a RIE etcher. The PMMA film is thick enough ($\sim$ 400-500 nm) to protect the graphene structures from being etched away by oxygen. Figure 7.2(a) shows the SEM image of graphene ribbon structures after the top PMMA layer is removed by acetone. The whole geometry of the graphene ribbon is 3.5 $\mu m$ $\times$ 50 $\mu m$. Multi voltage probes are located on both sides of this ribbon. To make top gated FETs, a 40 nm thick HSQ dielectric layer is patterned in a rectangular shape as an insulating layer on top of graphene devices. Finally, 60 nm thick Al top gates are lift-off deposited on the HSQ layer as shown in Figure 7.2(b). Al pads extend outside the HSQ region and connect with two graphene pads as labeled G in Figure 7.2(a). Hence, external top gate voltages are applied to Al pads through these two graphene pads. A schematic cross-section view of the whole device is illustrated in Figure 7.2(c).

### 7.3.2 Side Gated FETs

The original idea of side gated graphene FETs is to laterally adjust the density of carriers in the whole graphene layers and to avoid the screening effect from top graphene layers. In

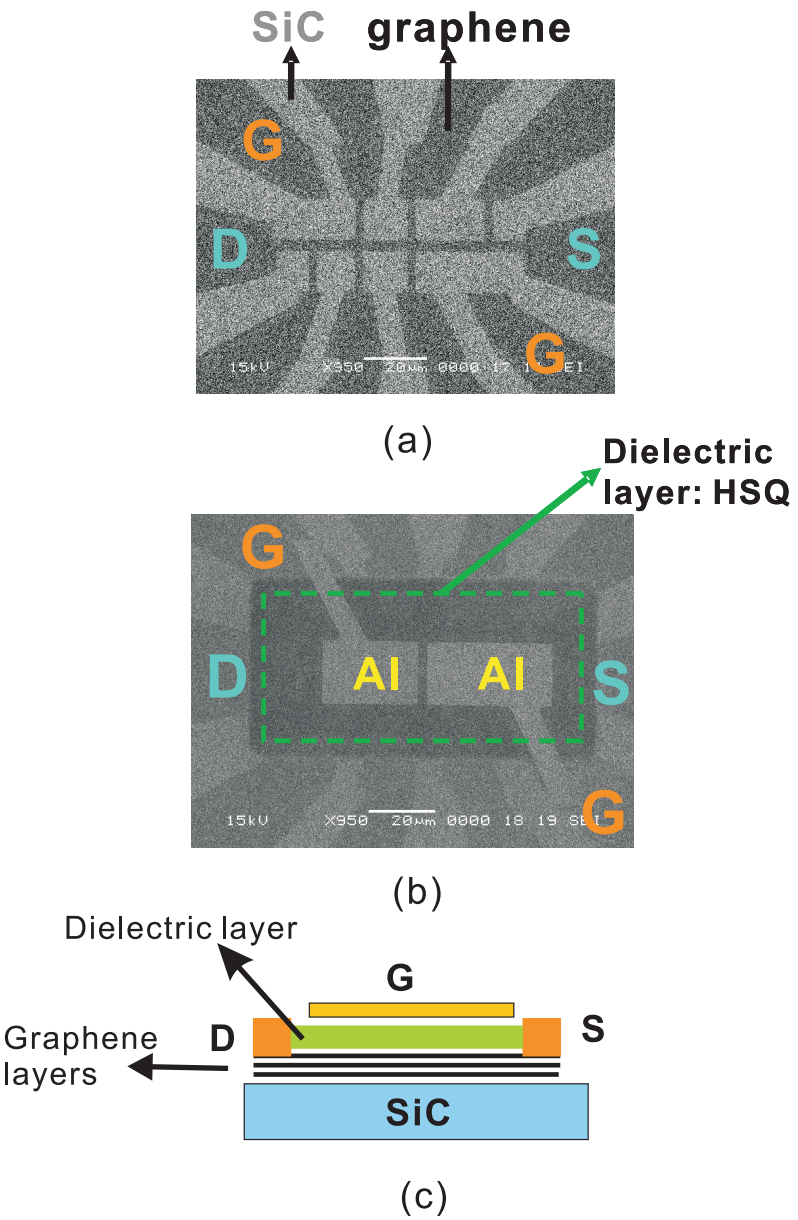


**Figure 7.2:** Images of top gated graphene FETs. (a) The SEM image of a graphene ribbon structure (3.5 $\mu m \times$ 50 $\mu m$) after plasma oxygen etching. Note: Two graphene pads (labeled G) are reserved to connect to the top gates. (b) The SEM image of top gated graphene FETs. Two separate Al top gates are deposited on a 40 nm thick dielectric HSQ film and are connected to two graphene pads in (a). (c) The schematic cross-section view of top gated graphene FETs.

side gated FETs, the insulating layer between the narrow graphene conducting channel and side gates should be very narrow to provide a strong external lateral electric field that can modify significantly the carrier density of the graphene conducting ribbon channel. Also, the graphene conducting channel should be narrow enough to induce an observable bandgap ($E_g \sim 1/\mathrm{W}$) caused by the ribbon width (W) restriction.

The fabrication of side gated FETs is not trivial on epitaxial graphene. It requires a careful design and a delicate processing work. By E-beam lithography, a high-resolution narrow ribbon can be defined by two narrow trenches in a thin PMMA film on top of epitaxial graphene. But thin PMMA is easily etched away by oxygen plasma etching. To protect the graphene regions coated with PMMA, we can either increase the thickness of PMMA layer with a lower pattern resolution or coat another etch metal on top of the thin PMMA layer. Here two approaches have been tried to fabricate side gated graphene FETs with narrow conducting ribbon channels and narrow insulating trenches. Approach A chooses a PMMA-metal bilayer as etch mask. Approach B chooses a thick PMMA as etch mask. With great efforts, we successfully fabricated side gated FETs by Approach A. Approach B has not given us very good results yet. The specific processing of these two approaches are described below.

#### *7.3.2.1 Approach A: PMMA-metal bilayer etch mask*

Approach A chooses the PMMA-metal bilayer as etch mask to fabricate side gated FETs. The process flow of approach A is listed below. The process scheme is show in Figure 7.3 (a).

1. Plane epitaxial graphene growth on a 3.5 mm × 4.5 mm 4H-SiC piece.

2. Deposition of metal contact Pd/Au (5 nm/100 nm) by an E-beam evaporator. (Base pressure: $2\times10^{-6}$ torr; evaporation rate: Pd (1Å per second), Au (1-1.5Å per second)

3. 1st PMMA spin coating and baking. (7 % PMMA, spin speed: 5 k RPM; baking: 180°C for 60 seconds)

4. 1st E-beam patterning (2 steps) on PMMA to define graphene big cross structures.

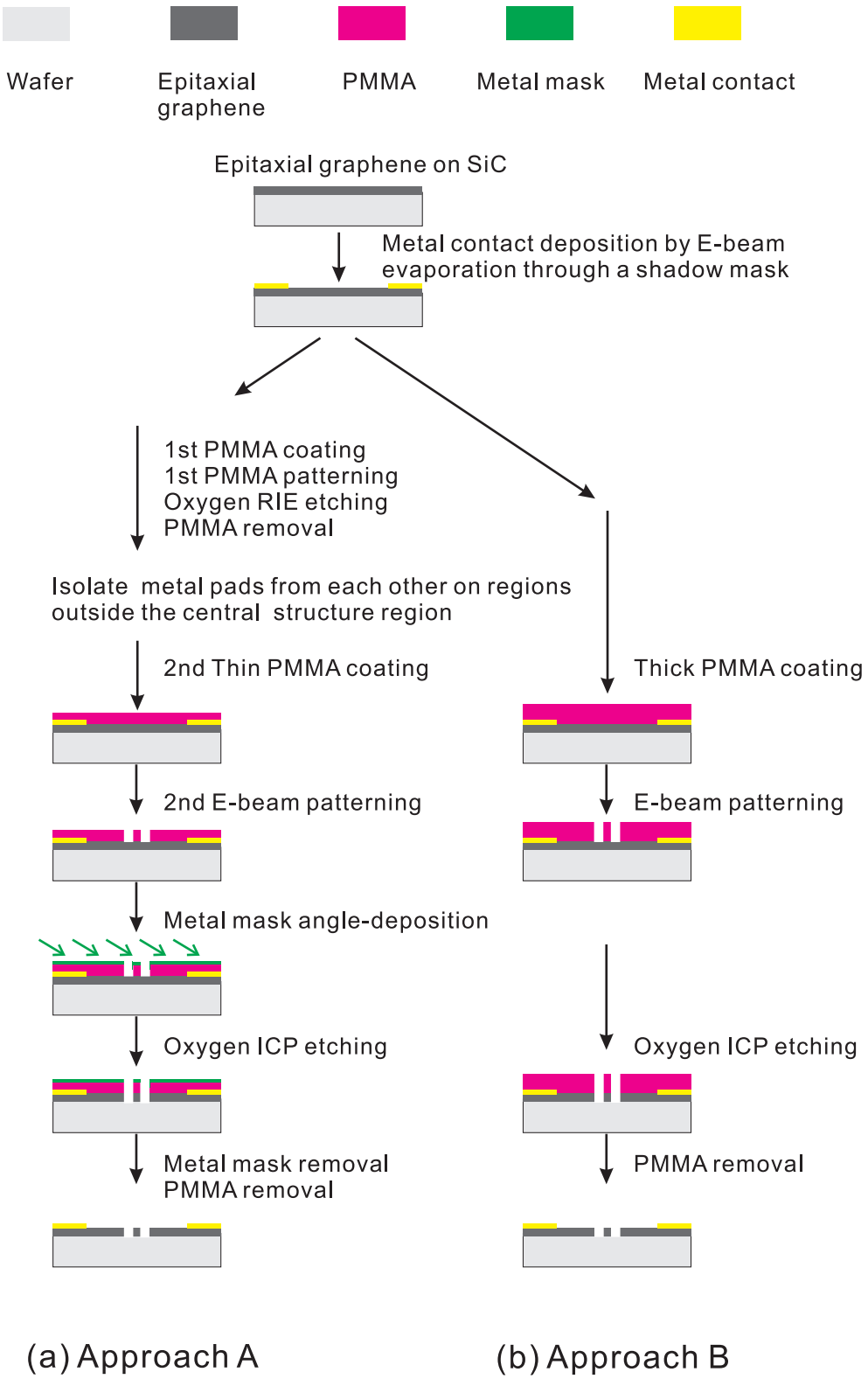


**Figure 7.3:** Fabrication processes of side gated graphene FETs. (a) Approach A: PMMA-metal etch mask. (b) Approach B: thick PMMA etch mask.

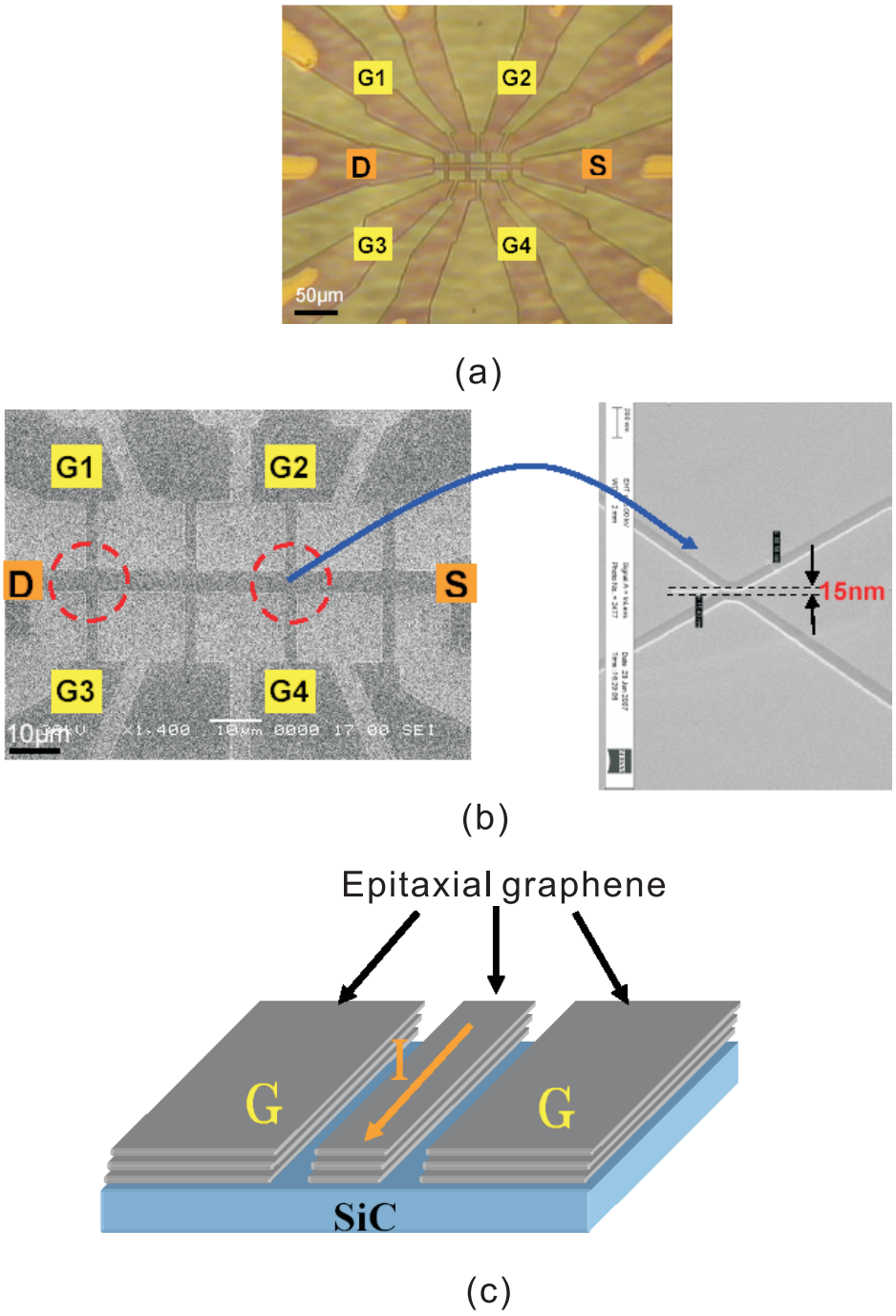


**Figure 7.4:** Approach A: images of side gated graphene FETs processing. (a) Optical image of graphene ribbon structures after 1st PMMA E-beam patterning and the RIE oxygen plasma etching. Note: PMMA is still left on top of graphene. Four vertical graphene ribbons are used later as side gates (G1, G2, G3, and G4) that are biased on the narrow graphene conducting channel from both sides. (b) SEM image of side gated graphene FETs after 2nd PMMA E-beam patterning. PMMA is still on the surface. Images are taken before the angle deposition of metal etch mask and the ICP etching. (c) The scheme of a side gated graphene FET.

5. Oxygen RIE etching. (Power:100 W; pressure: 100 mtorr; flow rate: 20 sccm; etching time: 60 seconds)

6. PMMA removal with acetone or Microposit remover 1165.

7. 2nd PMMA spin coating and baking. (3 % PMMA, spin speed: 10 k RPM; baking: 180°C for 60 seconds)

8. 2nd E-beam patterning on PMMA to define narrow trenches between the graphene conducting channel and graphene side gates. (Acceleration voltage of electron: 100 kV; dosage: 8000-9000 $\mu C/cm^2$)

9. Angle deposition of a thin Pd/Au (3 nm/7 nm) metal mask by an E-beam evaporator. (Base pressure: $2 \times 10^{-6}$ torr; evaporation rate: Pd (1.0Å per second) and Au (1.0-1.5Å per second))

10. Oxygen ICP etching. (Platen power: 50 W; coil Power:100 W; pressure: 10 mtorr; flow rate: 20 sccm; etching time: 30 seconds)

11. Pd/Au removal.

12. PMMA removal.

13. Wire-bonding and preliminary electrical test.

Approach A includes two E-beam patternings, two metal depositions, two resist spin coatings, two resist development, one RIE etching, and one ICP etching. For the two E-beam patterning processes, the 1st one is to remove the PMMA between metal pads on the regions except for the central region that is reserved for the 2nd E-beam patterning. After the oxygen RIE etching, the metal pads are isolated from each other except for the center region. Figure 7.4(a) shows the optical image of the whole graphene ribbon structures after the 1st E-beam patterning and the oxygen RIE plasma etching. After the removal of the thick PMMA layer (about 200 nm thick) as seen in Figure 7.4(a), the side gated structures are fabricated in the center region as described below. A 70 nm thick PMMA resist is

spin-coated on the surface. E-beam patterning defines two narrow trenches that are located between graphene ribbon channel and graphene side gates. Figure 7.4(b) shows the SEM images taken after the 2nd E-beam patterning and PMMA development. The graphene ribbon channel can be patterned as narrow as 15 nm, and the gaps between the channel and side gates are about 20-30 nm. To improve the PMMA etching resistance, a 10 nm thin metal mask (Pd/Au) is deposited on top of the PMMA layer at a angle of 45 degree from the normal surface of metal sources. No metal coats on the bottom of two narrow trenches. Then the sample is etched by oxygen plasma in an ICP etcher. Graphene layers on the bottom of trenches are etched away while graphene layers on the rest areas are protected by a bilayer etch mask: 70 nm PMMA + a 10 nm metal mask of Pd/Au. Finally, the metal layer and the PMMA layer are removed in sequence and only graphene side gated structures are left on the surface. The graphene conducting channel and side gates are only electrically isolated by air in the trenches and the non-conducting SiC substrate. Figure 7.4(c) shows the scheme of a side gated FET.

#### *7.3.2.2 Approach B: thick PMMA etch mask*

Approach B chooses the thick PMMA layer as etch mask to fabricate side gated FETs. The process flow of Approach B is listed below. The process scheme is show in Figure 7.3(b).

1. Plane epitaxial graphene growth on a 3.5 mm × 4.5 mm 4H-SiC piece.
2. Deposition of metal contact Pd/Au (5 nm/100 nm) by an E-beam evaporator. (Base pressure: $2\times10^{-6}$ torr; evaporation rate: Pd (1.0 Å per second), Au (1.0-1.5Å per second))
3. E-beam resist PMMA spin coating and baking. (3% PMMA; spin speed: 5-7 k RPM; baking: 180°C for 60 seconds)
4. E-beam patterning on PMMA to define graphene side gated structures.
5. ICP etching with pure oxygen. (Power: 100 W; pressure: 100 mtorr; flow rate: 20 sccm; etching time: 60 seconds)

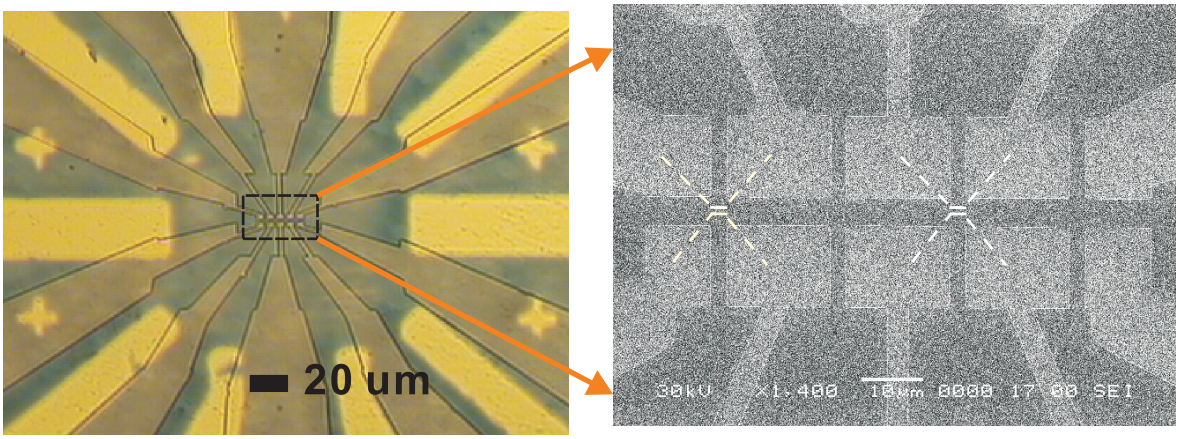


**Figure 7.5:** Approach B: images of side gated graphene FETs. The design of side gated structures is similar to that in approach A. (a) Optical image taken after E-beam patterning. PMMA is still left on top of graphene. (b) SEM image on the central region of side gated FETs. The added white broken lines mark where trenches are.

6. PMMA removal.

7. Wire-bonding and preliminary electrical test.

Approach B provides a simple process procedure: one E-beam patterning, one metal deposition, one resist spin coating , one resist development, and one ICP etching. A 130 nm thick PMMA resist is spin-coated on the surface of epitaxial graphene. The side gated FET structures are E-beam patterned on PMMA. Figure 7.6(a) shows the optical image of side gated FETs after the PMMA development. Later the sample is etched by pure oxygen plasma in an ICP etcher. The thick PMMA film protects graphene structures from etching. After the PMMA film is removed with acetone, graphene side gated structures are ready for test. The crucial process is the ICP etching. As etch mask, PMMA has poor resistance to oxygen plasma etching. A thinner PMMA film cannot protect the graphene devices very well. A thicker PMMA film can have a better protection on graphene devices but reduces the resolution of patterned narrow trenches. Besides that, the width of the trench becomes wider after ICP etching. To make a good side gated device, all these issues have to be considered during fabrication.

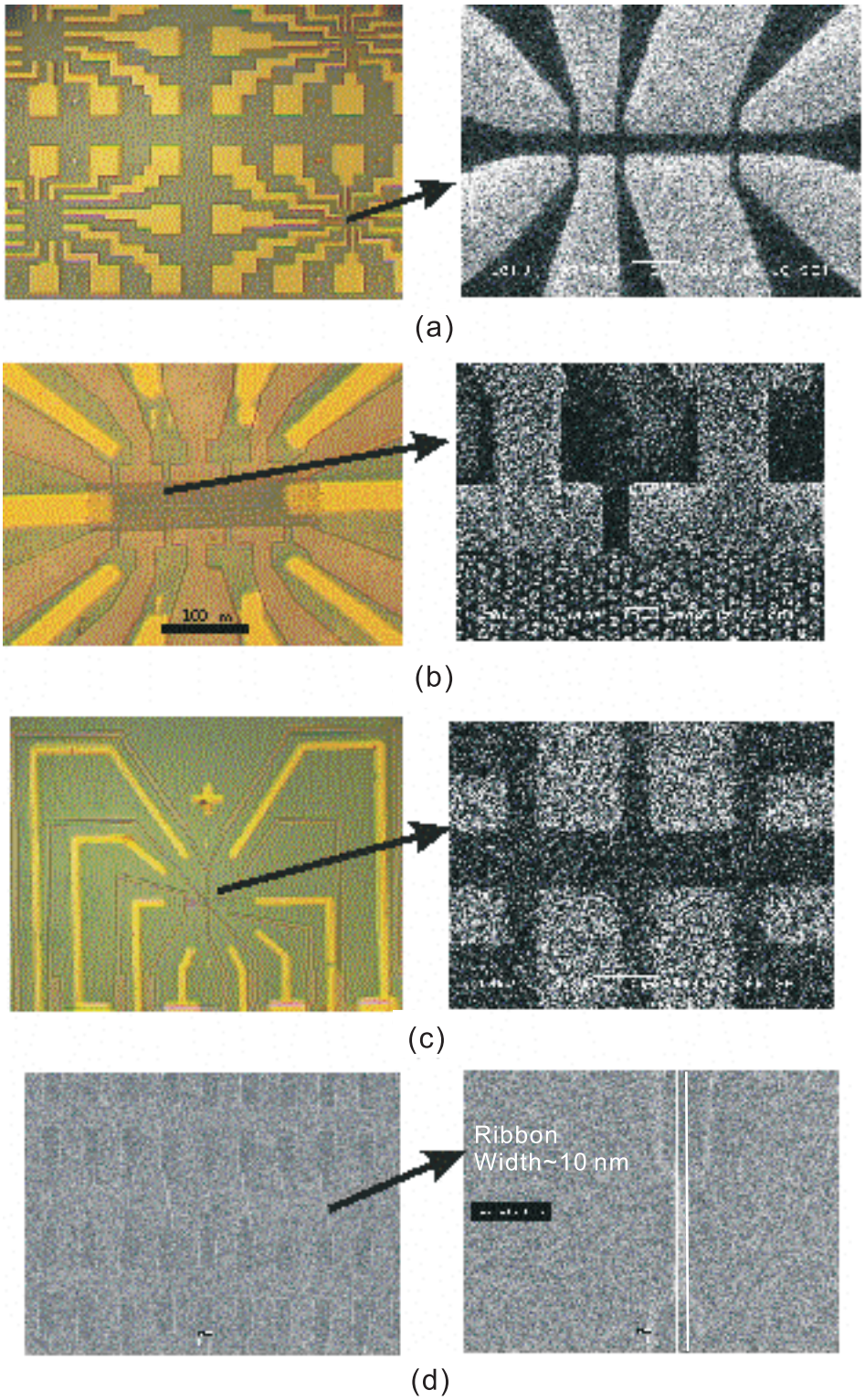


**Figure 7.6:** Examples of epitaxial graphene devices. For (a)-(c), the left is optical images and the right is SEM images after etching. (a) Multiple graphene structures integrated on a sample. Different graphene devices can be fabricated in the center of each structure. (b) Meshed graphene Hall bars. (c) Single side graphene structures for AFM lithography and EFM study. (d) HSQ patterning on epitaxial graphene film. The minimal width of HSQ ribbons is about 10 nm.

### 7.3.3 Other Epitaxial Graphene Devices

Besides graphene FETs, I also have fabricated other epitaxial graphene structures to study their transport properties. For example, standard graphene Hall bars are fabricated and measured to understand the magnetotransport properties of epitaxial graphene. Meshed Hall bars are used to study the disorder effects on graphene transport. Single-side graphene structures are used for AFM lithography and EFM (electrostatic force microscope) study by the tool of Veeco CP-II AFM/STM. Different shadow masks and photomasks are designed and fabricated to meet the requirements of different graphene projects. Figure 7.6 shows several typical structures that demonstrate the great potential and flexibility of epitaxial graphene in device fabrication.

## *7.4 Conclusion*

Epitaxial graphene on SiC is a 2D system. Epitaxial graphene can be fabricated into various devices by standard lithography and processing techniques. The fabrication of top gated graphene FETs and side gated FETs are described in detail.

# CHAPTER VIII

# TRANSPORT PROPERTIES OF EPITAXIAL GRAPHENE

Most of our transport measurements are done on epitaxial graphene films grown on quasi-insulating SiC substrates. Because of the work function difference (0.3 eV) between graphene and SiC, the bottom interface graphene layer is charged with an electron carrier density ranging from $10^{12}$ to $10^{13}/cm^2$, while the other top layers are quasi-neutral with a carrier density of $< 10^{10}/cm^2$. The infrared Landau level spectroscopy has probed the Dirac properties of carriers in the low density layers, while transport measurements have probed the Dirac properties of carriers in the high density bottom layer. This chapter will summarize the main results from infrared Landau level spectroscopy and magnetotransport experiments. The electric field effect on epitaxial graphene is realized on both top gated and side gated FETs.

## *8.1 Landau Level Spectroscopy*

The infrared Landau level spectroscopy experiment was performed on epitaxial graphene on the C face of 4H-SiC in a magnetic field at a low temperature by Sadowski et al. in the Grenoble High Magnetic Field Laboratory, CNRS, France [186, 187]. For massless Dirac particles in an external magnetic field, the Dirac energy spectrum evolves into discrete Landau levels with energies $E_n = V_F\sqrt{2\hbar eB\,|n|}$, where n is Landau level index [186]. The square root B dependence uniquely distinguishes massless Dirac particles from massive carriers in normal metals and semiconductors that have a linear B dependence of Landau level energies. In the infrared transmission spectrum as shown in Figure 8.1(a), the absorption peaks A, B, C, and D correspond to different transitions ($L_m \rightarrow L_n$) between Landau levels $L_m, L_n$ as indicated by the inset in Figure 8.1(a). The allowed transitions are only between adjacent Landau levels, and the transition energy is

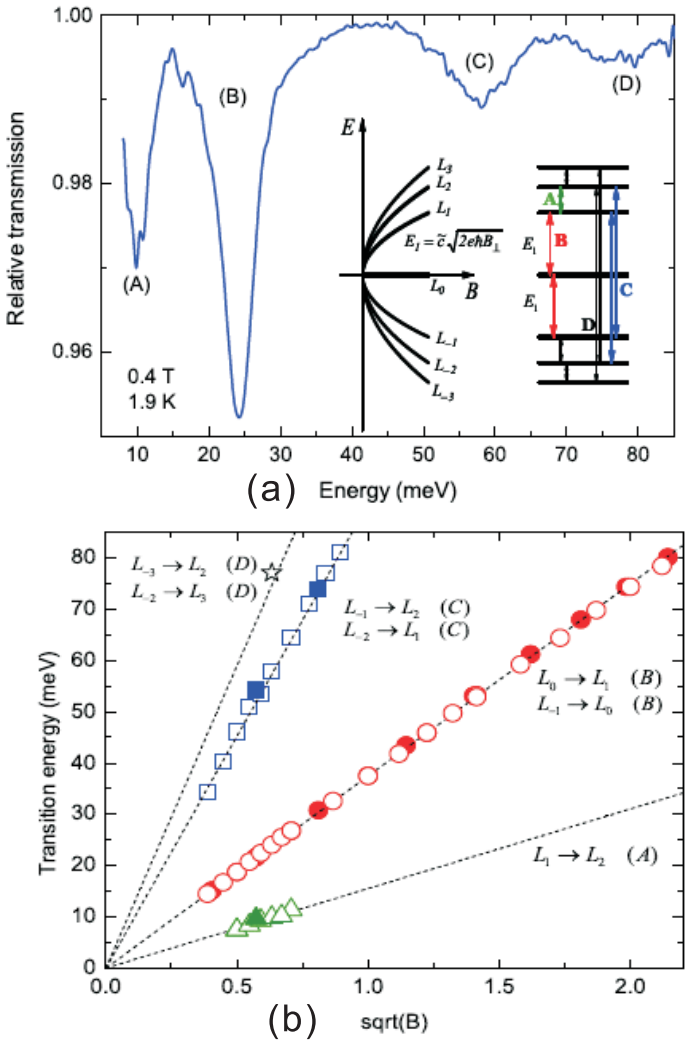


**Figure 8.1:** Landau level spectra of epitaxial graphene on the C face of the insulating 4H-SiC.(a) Infrared transmission at a magnetic field B = 0.4 T and temperature T = 1.9 K. The various absorption dips correspond to inter-Landau level transitions as indicated in the energy level diagrams. (b) The square root B dependence of the transition energies of the various transitions demonstrates this characteristic graphene property. Note that for normal materials the field dependence is linear [186, 187].

$$\Delta E_n^t = V_F\sqrt{2\hbar eB}\left(\sqrt{|n+1|} \pm \sqrt{|n|}\,\right) \tag{8.1}$$

The spectrum can not tell the difference between $L_n \rightarrow L_{n+1}$ and $L_{-(n-1)} \rightarrow L_{-n}$ since they have the same transition energies [187].

Figure 8.1(b) plots out the square root B dependence of different transition energies, and reveals the Dirac-particle nature in multilayer epitaxial graphene. From the equation 8.1, the effective velocity is found to be $V_F = 1.03 \times 10^6 m/s$ that is very close to the Fermi velocity measured in exfoliated graphene. The transition between $n = 0$ and $n = 1$ is only observed for B$>$ 0.15 T, which implies that the carriers in the $n = 1$ level are completely depleted at B=0.15T. Hence, the Fermi energy is in the range of $-15meV < E_F < 15meV$. The upper limit to the carrier concentration in the observed graphene layers is $n_s = \frac{4k_F^2}{4\pi} < 2.1 \times 10^{10}/cm^2$. All these carriers are believed to originate from the less doped top layers [186, 187].

## *8.2 Transport Properties of Epitaxial Graphene*

Magnetotransport properties of epitaxial graphene films have been measured either on the Si face of 6H-SiC or on the both faces of 4H-SiC in the magnetic field range of from -9 T to 9 T (even -23 T to 23 T) and in the temperature range from 2 K to 300 K. Different graphene devices are fabricated with sizes of hundreds of micrometers to tens of nanometers either by photo- or by E-beam lithography. Most transport measurements are done on the C face of 4H-SiC. As shown later, carriers in epitaxial graphene grown on the Si face (in UHV) have a lower mobility compared to those on the C face (in our growth system).

From experimental analysis, epitaxial graphene on SiC possesses the following important properties [17, 18, 19, 40, 237]:

1. Anomalous Berry's phase,
2. Square root B dependence of Landau level,
3. Weak anti-localization,
4. Long phase coherence length ($\sim \mu m$),

5. Quantum confinement on narrow ribbons (<500 nm).

Besides these properties, the mobility of carriers does not degrade with the shrinkage of the ribbon width. The anomalous quantum hall effect (QHE) phenomenon has not been observed on epitaxial graphene. These phenomena will be discussed below.

### 8.2.1 Shubinkov de Haas (SdH) Oscillations and Weak Anti-localization (WAL)

A wide graphene ribbon of 100 $\mu m$ wide is patterned on the C face of an insulating 4H-SiC (as in Figure 8.2). The magnetoresistance (MR) measurements on this sample reveal both SdH oscillations and weak anti-localization phenomena [237].

Figure 8.2(a) shows a series MR plots recorded at several temperatures. The resistance increases with magnetic field. Each MR plot can be pictured as a combination of a large MR background and the tiny SdH oscillations. This large, positive MR background is attributed possibly to the top graphene layers with a low carrier density $n \sim 10^{10}/cm^2$. The tiny SdH oscillations are attributed to the interface graphene layers with a charge density of 3.8 $\times 10^{12}$ electrons $/cm^2$. The left inset in Figure 8.2(b) shows small SdH oscillations after the linear MR component is subtracted as a background at 4.2 T. These oscillations are periodic in 1/B, which is characteristic of the quantum mechanical Shubinkov de Haas (SdH) effect caused by the quantization of the cyclotron orbits. The oscillation period (in 1/B) is determined by the carrier density that is hence found to be $3.8 \times 10^{12}/cm^2$. The phase of the oscillations (in 1/B) is determined from a Landau plot which plots the MR peak positions versus 1/B. The phase is then determined by the intercept with Y-axis by a linear fit in Figure 8.2(b). The phase is found to be near zero and is consistent with an anomalous Berry's phase $\Phi = \pi$, characteristic of Dirac particles. (For normal metals and semiconductors, the Landau plot intercepts the Y-axis at 1/2, and the Berry's phase is $\Phi = 0$.) The temperature dependence of SdH magnetoresistance amplitudes is described by the Lifshitz-Kosevich equation $A_n(T) \sim u/sinh(u)$, where $u = 2\pi kBT/\Delta E(B)$. The expected Landau level spacing for Dirac particles $\Delta E_n(B) = E_{n+1} - E_n$ fits this equation well [237].

Moreover, after the subtraction of a temperature independent background, the low field

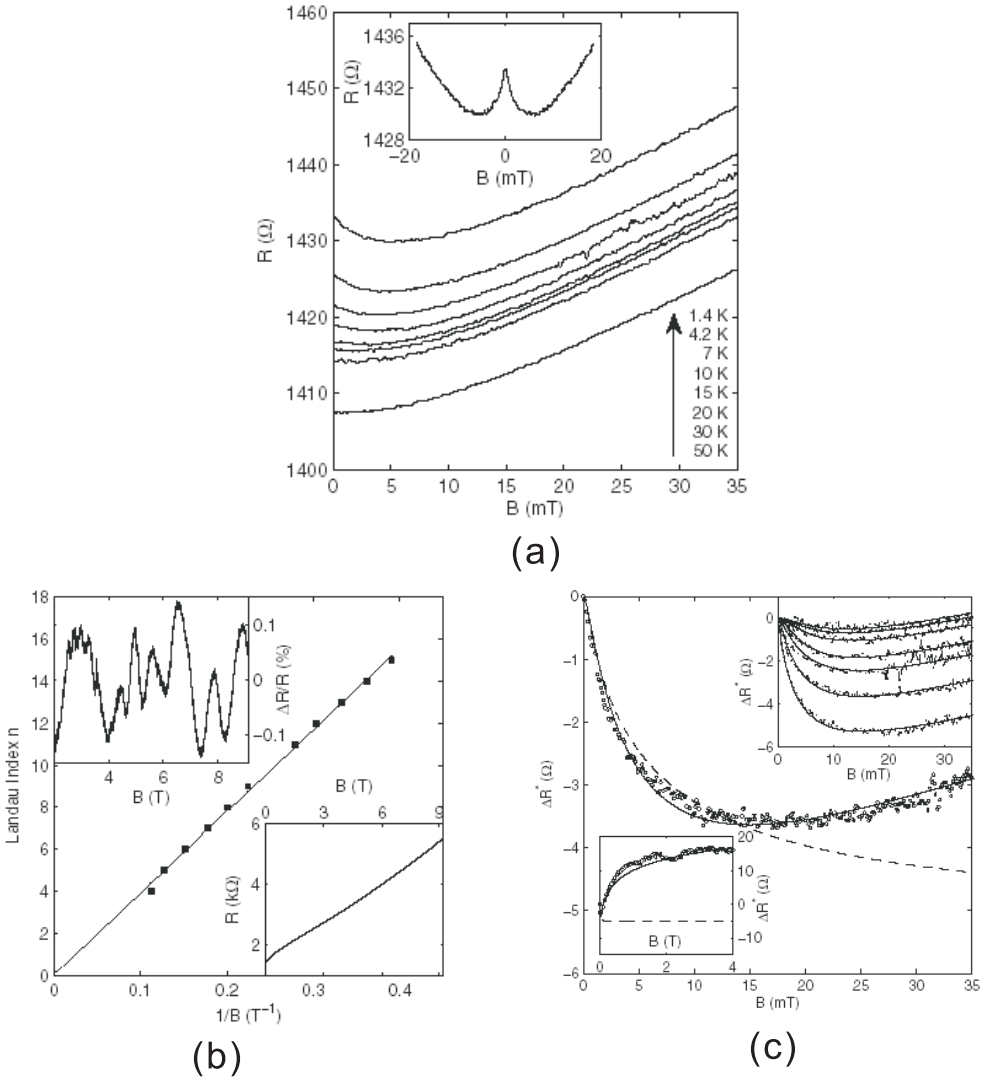


**Figure 8.2:** Magnetoresistance (MR) study of a 100 $\mu m$ wide epitaxial graphene ribbon. (a) MR plots at various temperatures. The inset: the magnetoresistance peak near B = 0 T can be seen when sweeping the field from -20 mT to 20 mT at 1.4 K. Mobility $\mu = 11,600 cm^2/Vs$. (b) Landau plot (Landau index n vs 1/B) of SdH oscillation peaks up to 9 T at 4.2 K (solid square). The solid line corresponds to a linear fit that gives a magnetic frequency of 39 T and an intercept of 0.03 ± 0.17 on the n axis. Right inset: resistance as a function of B at 4.2 K. Left inset: small SdH oscillations after subtraction of the quadratic MR background from the resistance curve plotted in the right inset. (c) Fit of the low-field $\Delta R^*$ at 4.2K after the quadratic MR background subtraction. The fit shows the characteristic graphene weak anti-localization behavior. Open circles are the data. Dashed line is a fit to the weak localization theory for a normal 2D metal. An acceptable fit can be obtained only below 20 mT. Solid line is a fit to the WAL model by McCann et al. [122]. The fit shows good agreement for the entire range of field. Right inset: dash-dotted line, $\Delta R^*$ for T = 1.4 K, 4.2 K, 7 K, 10 K, 15 K, 20 K, and 30 K from bottom to top; solid line fits McCann's model. Left inset: plot of the main panel extended to 4 T [237].

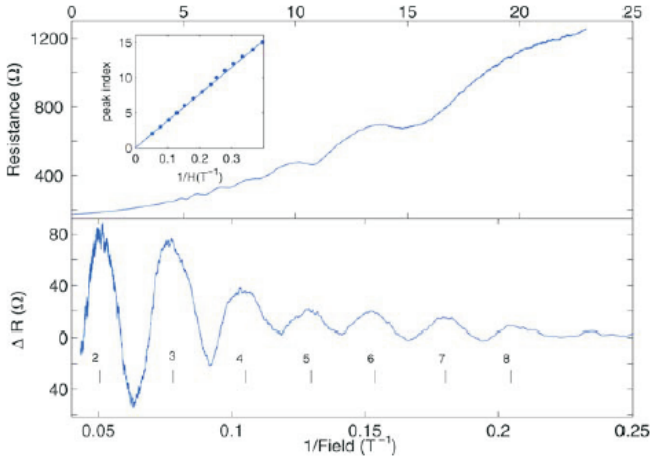


**Figure 8.3:** Top panel: Square resistance $\rho_{xx}$ as a function of magnetic field at 180 mK showing the SdH oscillations. Bottom panel: $\rho_{xx}$ with a smooth background subtracted. The magnetoresistance peaks at $B_n$ are labeled with their Landau level index n. Inset: Landau plot: n versus $1/B_n$ is a straight line, which intercepts the Y-axis at $\gamma < 0.1$, consistent with a Berry phase $\Phi = \pi$, the slope gives a carrier density $n_s = 3.7 \times 10^{12}/cm^2$ [18].

$\Delta R^*$ shows a very small peak around B = 0 T, and an upturn at B > 0.02 T (see Figure 8.2(c)). All features are well explained and fitted by the weak anti-localization theory that originates from the characteristics of massless Dirac particles in graphene [122, 237]. Dirac particles have a chiral nature that originates from the equivalence of A,B sublattices on a graphene sheet. The term pseudospin is assigned to describe this chirality. Pseudospin is coupled with the direction of the momentum. In order to reverse the direction of momentum by scattering, the pseudospin has to be reversed at the same time. However, intravalley scattering (or long-range scattering) between A and B cannot reverse the value of pseudospin because of the equivalence of A,B sublattices. Thus, direct backscattering is not inherently favorable in clean graphene unless intervalley scattering happens by the involvement of more short-range defects [237].

A high field ($\sim$ 23 T) magnetoresistance measurement on a $1\mu m \times 5\mu m$ graphene Hall bar on the C face of 4H-SiC also provides clear SdH peaks and similar weak anti-localization properties as seen in Figure 8.3 [18].

Transport properties of graphene films on the Si face of conducting 6H-SiC were also investigated as shown in Figure 8.4. This sample was graphitized in UHV and about 2-3

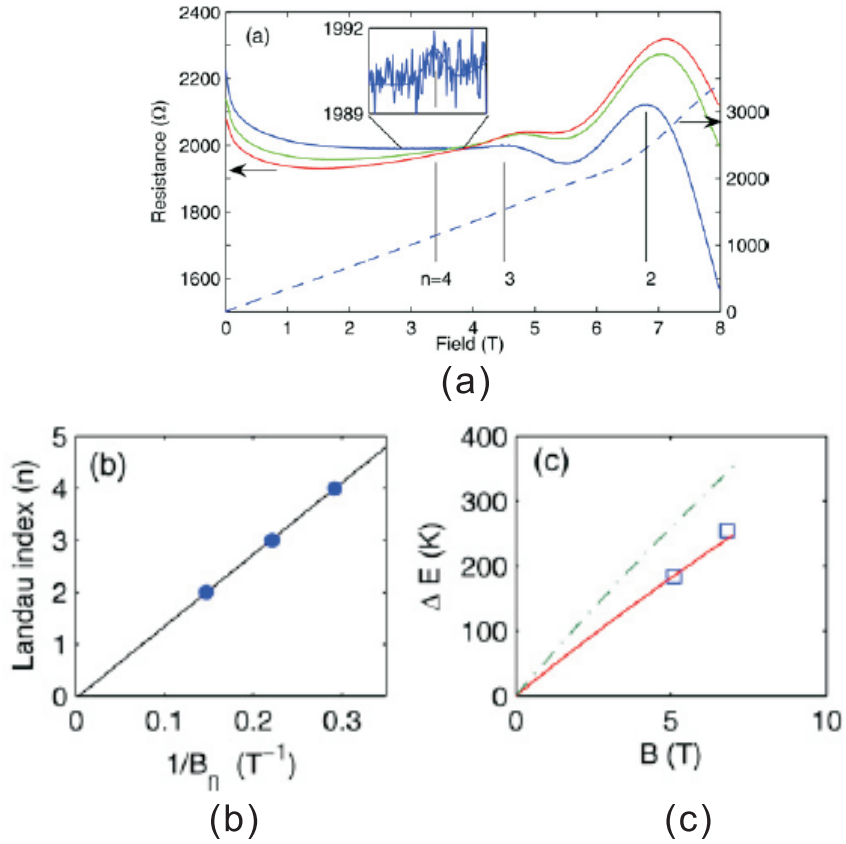


**Figure 8.4:** Magnetoresistance transport measurements in a 400 $\mu m \times$ 600 $\mu m$ Hall bar on 2-3-layer epitaxial graphene on the Si face [17]. Mobility $\mu = 1200 cm^2/Vs$, coherence length $l_\varphi = 300$ nm. (a) Magnetoresistance at T = 0.3, 2 and 4 K showing well developed SdH peaks that are indicated with their Landau indices n; the Hall resistance at 0.3 K (dashed line), shows a weak feature at the expected Hall plateau position. The amplitude of the weak localization peak at B = 0 corresponds to 1 $G_0$. (b) Landau plot. The linear extrapolation passes through the origin, demonstrating the $\pi$ Berry's phase characteristic of graphene. (c) The Lifshitz-Kosevich analysis of the n = 2 and n = 3 peaks that correspond to graphene with a Fermi velocity $V_F = 7.2 \times 10^5 cm/s$ [40].

graphene layers were grown on the Si face of 6H-SiC. A 400 $\mu m\times$ 600 $\mu m$ Hall bar was patterned and measured in the magnetic field of 0 T to 8 T in the temperature range from 4 K to 50 K. The carriers in the SiC substrate are frozen at temperatures below 50 K. Similar to graphene on the C face, SdH oscillations are observed on the Si face with high-quality graphene. The carrier motilities (1,120 $cm^2/Vs$) are about one order magnitude lower than those on the C face. The Landau plot also indicates the anomalous Berry's phase, the Dirac nature of carriers.

However, Hall resistance measurements on different wide graphene ribbons on the C face do not show clear evidences for the QHE observed in other 2D material systems. The pronounced SdH oscillations and the trace of quantum Hall plateaus are shown on graphene ribbons on the Si face where epitaxial graphene films have more defects and lower mobility ($\sim$ 1,000 $cm^2/Vs$) than those on the C face ($\sim$ 27,000 $cm^2/Vs$). Thus the missing of the QHE may be due to some defect-related reasons or to some unique properties in this multilayer graphene-SiC system [40].

### 8.2.2 Long Phase Coherence and Quantum Confinement

Epitaxial graphene on the C face of 4H-SiC has a long phase coherence length [19, 18, 40, 237]. Measured from multiple epitaxial graphene samples on the C face of 4H-SiC, the phase coherence length is about $L_\phi = 1.1\ \mu m$ at 4 K [19]. For the epitaxial graphene grown on the Si face of 6H-SiC in UHV, the phase coherence length is about 300 nm [17]. When the length of a graphene ribbon is less than $L_\phi$, an electron can pass through the ribbon without losing its phase coherence. This reveals the potential of epitaxial graphene in phase coherent device applications.

Quantum confinement in epitaxial graphene was observed on a $0.5\mu m \times 6\mu m$ ribbon [19]. The confinement effect is apparent at low magnetic fields for narrow ribbons when the cyclotron diameter ($\propto 1/B$) becomes comparable or larger than the ribbon width. Then the energies of Landau levels are modified by the quantum confinement and are approximately described by

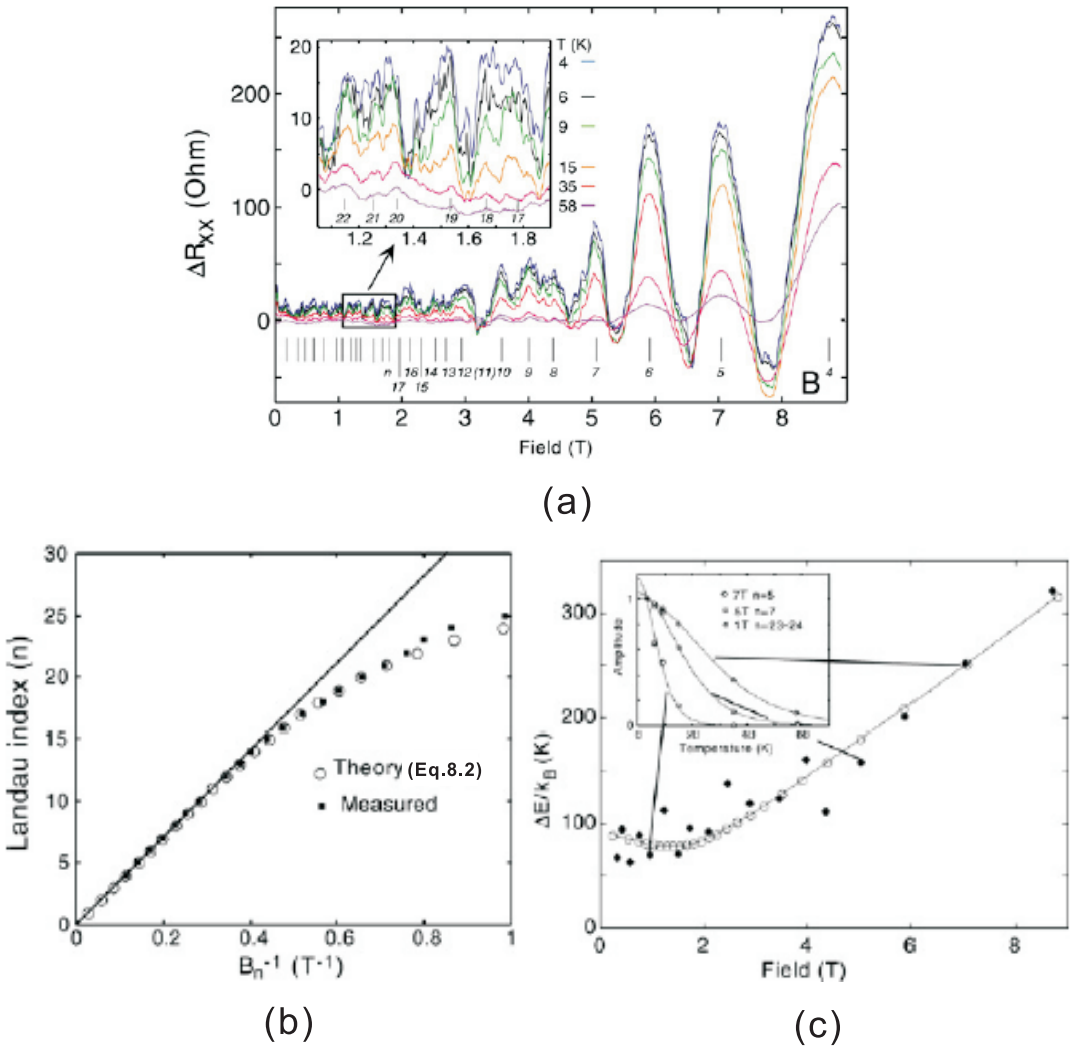


**Figure 8.5:** Narrow Hall bar 500 nm × 6 $\mu m$. The zero field resistance is 1125 Ω. (a) Magnetoresistance oscillations for temperatures ranging from 4 to 58 K after subtraction of a smooth background. (b) Landau plot of the magnetoresistance peaks. The deviation to large from linearity is due to quantum confinement. (c) The energy gap between the Fermi level and the lowest unoccupied Landau level is found from the Lifshitz-Kosevich analysis (inset) of the peaks and increases linearly with the field for large fields and saturates for low fields. The saturation confirms quantum confinement [19].

$$E_n(B,W) \approx \left[E_n^4(B) + E_n^4(W)\right]^{1/4}. \tag{8.2}$$

where $E_n(B) = \pm V_F\sqrt{2\hbar eBn}$ and $E_n(W) = n\pi\hbar V_F/W$ [173]. $E_n(B)$ is energies at the Landau levels due to quantization of cyclotron orbits in a magnetic field. $E_n(W)$ is the quantized energies due to quantum confinement by the narrow ribbon width. Consequently, the Landau levels at high fields evolve to the quantum confined levels at low fields as the magnetic field reduces. This causes the Landau plot to gradually deviate from the linear behavior for low fields.

## *8.3 Electric Field Effect on Epitaxial Graphene*

As previously discussed [17, 19, 40, 237], the transport properties of epitaxial graphene are dominated by carriers from the bottom graphene layer at the interface. Back gating of epitaxial graphene is difficult because there is no dielectric insulating layer between the SiC substrate and epitaxial graphene. For an insulating SiC substrate, one could choose the bulk SiC substrate itself as the dielectric spacer layer. But that demands a very delicate SiC wafer polishing and etching process to obtain SiC slices that are sufficiently thin, i.e less than 1 $\mu m$. In this thesis, top gated FETs and side gated FETs are fabricated on epitaxial graphene as described in Chapter VII. Few-layer and multi-layer graphene devices are fabricated and studied on either Si face or C face of insulating 4H-SiC substrates, respectively.

These FETs are measured at a temperature range from 4 K to 300 K with or without magnetic field. SR850 Stanford Research lock-in amplifiers are used to measure the potential drops between voltages probes located along the epitaxial graphene conducting ribbon channel. Keithley 2400 Sourcemeter is used to provide a DC gate and to monitor the possible gate leakage current.

### 8.3.1 Top Gating Effect

The top gating effect has been observed on epitaxial graphene ribbons on both the Si face (few graphene layers) and the C face (more graphene layers) of the insulating 4H-SiC.

For top gated graphene FETs on the Si face of 4H-SiC (sample 7D9), a 40 nm thick HSQ (hydrogen silsesquioxane) dielectric layer is spun and E-beam patterned on a 3.5 $\mu m$ $\times$ 12.5 $\mu m$ graphene ribbon. The epitaxial graphene film on sample 7D9 is 2-3 layers thick. A local top gate of Al is deposited on the top of this 40nm thick HSQ layer.

The external excitation current (the drain-source current) is constant at 10 nA. The DC gate $V_g$ sweeps between +10 V and -10 V. No gate leakage is observed during the measurement. The FETs were tested in a temperature range of 4 K - 300 K with and without magnetic field (from -9 T to +9 T).

Figure 8.6(a) shows the Hall resistance of the ribbon channel as a function of magnetic field under different $V_g$s at 4 K and 280 K. The total carrier density of the ribbon channel can be derived from the Hall measurement, $n_s = \frac{1}{eR_{hall}}$, where Hall coefficient is $R_{hall} = \frac{V_H}{IB}$ and $V_H$ is Hall voltage. It is clear that $n_s$ is inversely proportional to $V_H/IB$, the slope of the Hall resistance curve. Without the external electric field, $n_s$ is about $15.7 \times 10^{12}/cm^2$ at 4 K. Figure 8.6(b) shows that the carrier density changes with $V_g$.

Figure 8.6(c) is a plot of the change of carrier density $\Delta n_s = n_s(V_g) - n_s(V_g = 0)$. The estimated carrier density $n_{ind}$ induced by $V_g$ is also shown in Figure 8.6(c) as a comparison with $\Delta n_s$. From the capacitance calculation, $n_{ind}$ can be expressed as $n_{ind} = \frac{\epsilon_0 \epsilon_r V_g}{de}$, where $\epsilon_0$ is permittivity of the vacuum, $\epsilon_r$ is the relative dielectric constant, and $d$ is the thickness of the dielectric layer. $\epsilon_r$ is chosen to be 2.85 for HSQ [42] and $d$ is 40 nm. The $n_{ind}$ can be simplified to be $n_{ind} = \frac{15.77 \times 10^{12} V_g}{d}/cm^2$. We can see $n_{ind}$ and $\Delta n_s$ matches fairly well. The slight mismatch between them is caused possibly by the inaccuracy of dielectric layer thickness measurement and the selection of HSQ dielectric constant.

HSQ is a three-dimensional polymer with a cagelike network based on the empirical formula of $(HSiO_{3/2})_{2n}$ with $n$=2, 3, 4, .... HSQ can be pictured as the derivative of $SiO_2$ with three oxygens and one hydrogen bonded to each Si [42, 197]. HSQ films have been studied by several groups [34, 42, 111, 197, 220]. The properties, particularly dielectric properties, of HSQ are strongly influenced by different treatments such as thermal curing, radiation, and plasma annealing. For example, the redistribution of Si-O and Si-H bonds in HSQ was claimed to be the reaction mechanism responsible for the chemical change of

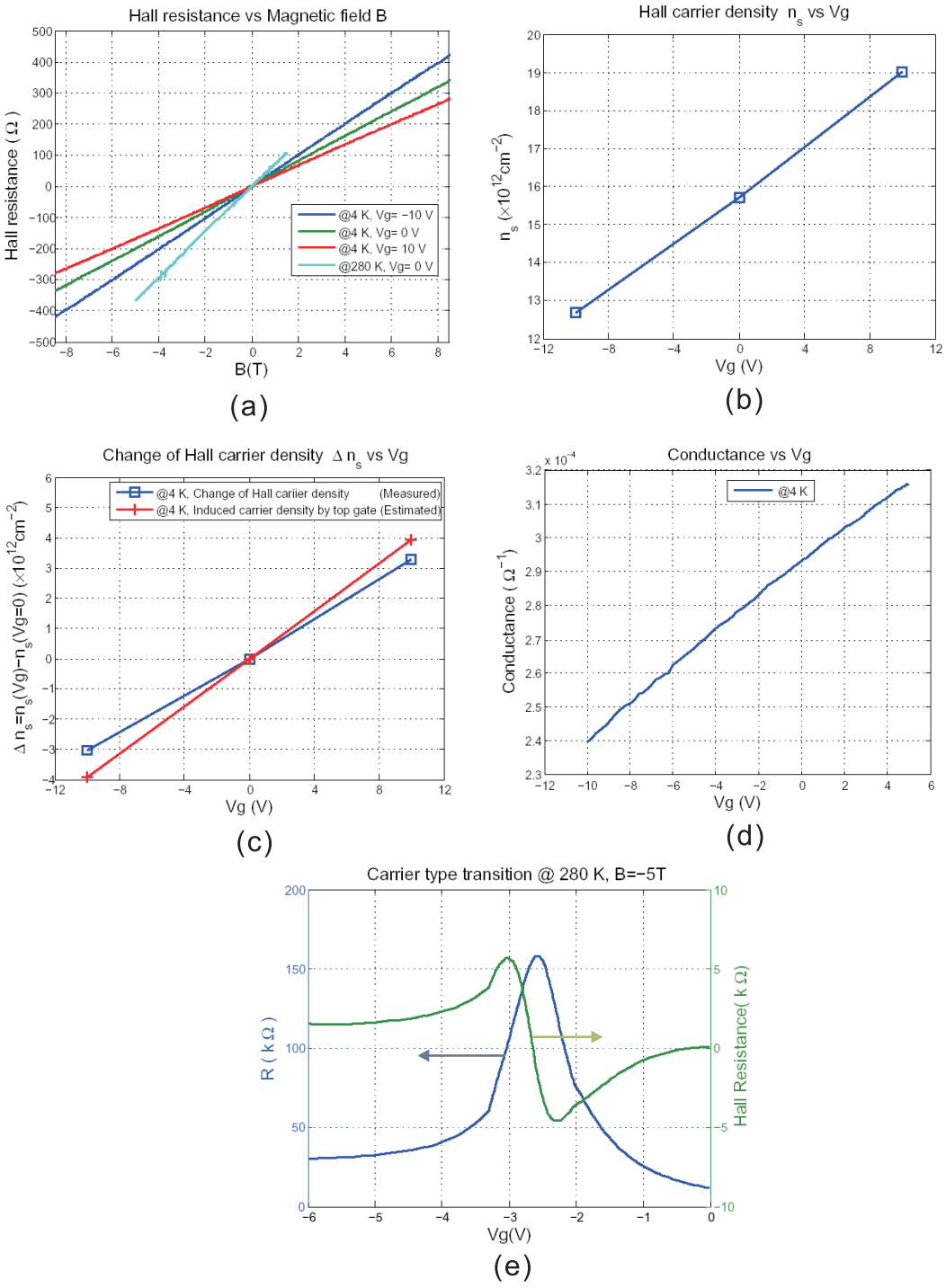


**Figure 8.6:** Top gating effect on a Si-face graphene FET (sample 7D9). Ribbon geometry: 3.5 $\mu m\times$ 12.5 $\mu m$). (a) The Hall resistance as a function of magnetic field. (b) The ribbon carrier density derived from (a) Hall measurement. (c) The comparison of carrier density between Hall measurement and capacitance calculation. (d) The channel conductance as a function of $V_g$ at 4 K. (e) The carrier type transition at 280 K.

HSQ during thermal curing [197]. For graphene FETs, HSQ has experienced spin coating, baking, E-beam patterning, and development. The whole process could modify the dielectric constant of HSQ.

Figure 8.6(d) plots out the channel conductance as a function of $V_g$ at 4 K. The minimum conductance has not been reached when $V_g$ sweeps from 5 V to -10 V. The Hall carrier density of 15.7 $\times 10^{12}/cm^2$ at $V_g = 0$ V requires a $V_g$ of about -40 V to reach the conductance minimum at 4 K.

At 280 K, a carrier type transition happens on this ribbon at $V_g$ = -2.6 V under $B$ = -5 T. In Figure 8.6(e), the resistance maximum of 160 k Ω is observed accompanying a clear sign switch of Hall resistance. This switch indicates a carrier type transition between electron and hole. The external electric field change the Fermi level $E_F$ either away from or toward to the Dirac point where the conduction band and the valence band touch. Once the $E_F$ passes the Dirac point, the carrier type is inverted. From the Hall measurement in Figure 8.6(a) , the carrier density at 280 K is about $8.79 \times 10^{12}/cm^2$, which requires a $V_g$ of more than 20 V to reach the Dirac point. Why does the maximum of resistance appear at $V_g$ = -2.6 V at 280 K? We suspect the mobile ions in HSQ plays an important role.

Devine, et al., demonstrated that negative and positive charges exist in the HSQ films [42]. In their study, the negative charges can be removed from the HSQ film by application of modest electric fields; positive charge can be similarly displaced but not removed from the film. That results in time dependent relaxation and the redistribution of the positive charge when the film is either unbiased or biased.

We assume that charged ions in HSQ are frozen at a low temperature (4 K), but become mobile at a high temperature (280 K) and redistribute themselves under an external electric field. For example, under a negative gate bias, positive ions may accumulate in a region near the top gate, negative ions may accumulate in a region near the ribbon channel. The built in electric field between the positively charged ions and negatively charged ions may counteract partially the external electric field so that HSQ merely mimics a high-k dielectric. As a result, the effective dielectric layer may be thinner than its physical thickness of 40 nm, which can explain why a lower top gate potential can reach the Dirac points at 280 K.

Below, I will discuss the top gating effect on epitaxial graphene on the C face of 4H-SiC.

One C-face graphene FET was made on sample 7B4. The epitaxial graphene film on sample 7B4 is about 10 layers thick. The graphene ribbon is 3.5 $\mu m$ wide and 12.5 $\mu m$ long. The HSQ dielectric layer is about 40 nm thick. The DC gate voltage $V_g$ sweeps between +12 V and -12 V. No gate leakage is observed during the measurement.

Figure 8.7(a) shows that the Hall resistance changes with the magnetic field B under different $V_g$s. Because the Hall probes are located outside the gated region defined by the top Al pad, Figure 8.7(a) does not provide an accurate Hall resistance under the influence of $V_g$. The carrier densities derived from the above Hall measurement in Figure 8.7(b) are not precise enough. Nevertheless, we still can analyze qualitatively the gating effect on the ribbon. The carrier density decreases as $V_g$ sweeps from -8 V to 8 V, which indicates that the graphene layers affected by external electric field are p-doped. As we know, for a clean epitaxial film, the interface graphene layer is n-doped while the top graphene layers are quasi-neutral. However, during the FET fabrication, impurities could be introduced at the interface between top graphene layers and the HSQ layer. These impurities could cause the top graphene layers to become p-doped.

Figure 8.7(c) shows the ribbon conductance as a function of $V_g$ at B = 0 T. The blue and red curves are measured at two different temperatures ( 4 K and 150 K). It also shows that the graphene layers that are affected by external electric field are p-doped. For the blue curve (4 K), when $V_g$ sweeps between +12 V and -12 V, the total carrier density in the ribbon channel is tuned. The minimum conductance is at around $V_g$ = 5 V. On the whole, the conductance of the ribbon can be changed by about 30% by sweeping $V_g$ between ± 12 V. For the red curve (150 K), the conductance minimum point is at around 2.6 V. The conductance of the ribbon is changed by more than 40% during the sweeping of $V_g$ between ± 12 V. The relative shift of the conductance minimum between 4 K and 150 K may be due to the combination of two possible effects. The first effect is the change of doping concentration from impurities at the interface when temperature changes from 4 K to 150 K. The second effect is related to the HSQ dielectric layer mentioned before. The effective HSQ dielectric layer is thinner than its physical thickness (40 nm). Under the same $V_g$, a

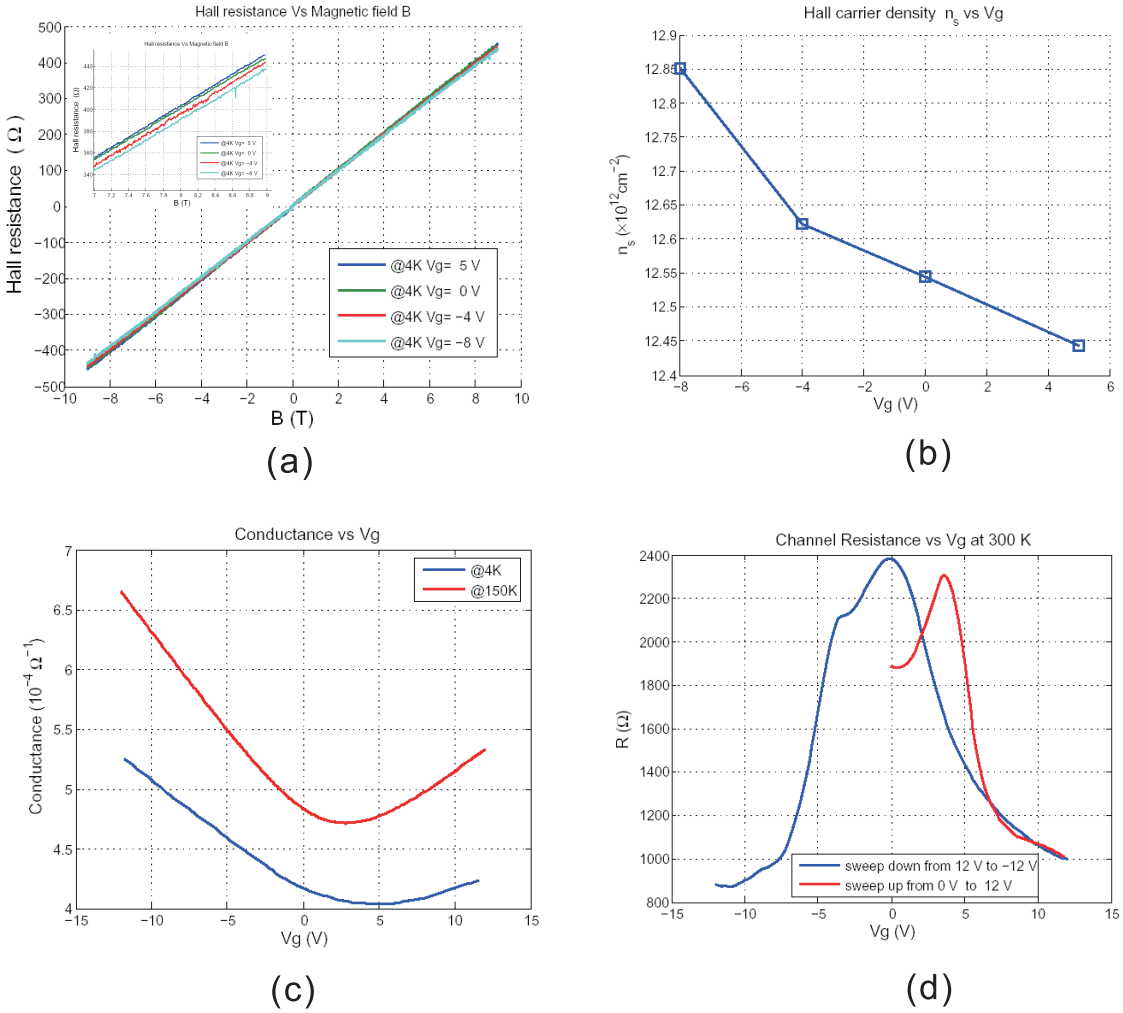


**Figure 8.7:** Top gating effect on a C-face graphene FET (sample 7B4). Ribbon geometry: 3.5 $\mu m\times$ 12.5 $\mu m$. (a) The Hall resistance as a function of magnetic field. Hall measurement at $V_g \neq 0$ is not accurate because the Hall probes are located outside the gating region. (b) The ribbon carrier density derived from (a) Hall measurement. (c) The channel conductance as a function of $V_g$ at 4 K and 150 K. (d) The hysteresis phenomenon of HSQ at 300 K. $V_g$ sweeps from 0 V to 12 V, then sweeps down to -12 V.

stronger electric field is applied on epitaxial graphene ribbon channel at 150 K than at 4 K. Therefore, a lower gate potential (2.6 V) could tune the ribbon conductance down to its minimum at 150 K.

The effect of ions in HSQ is more significant at a higher temperature. In Figure 8.7(d), the plot of $R$ Vs $V_g$ shows a huge hysteresis when $V_g$ sweeps from 0 V to 12 V, then back to -12 V at 300 K. (The hysteresis is not observed at low temperatures (such as 4 K).) The phenomenon of hysteresis is a serious problem in polymer based gate dielectrics (such as those used in organic FETs). The value of channel current ($I_{ds}$) depends on the direction of sweep of the gate voltage $V_g$. The hysteresis is attributed to the space charges (such as surface charges and mobile ions) that accumulate at the interface between the dielectric layer and the channel. Particularly, it is not easy to remove mobile charges completely from the polymer because the ions entangle with the polymer chains [222]. To have a more controllable gating effect on epitaxial graphene, better dielectric material (such as $HfO_2$ and $Al_2O_3$) is required to avoid the above problems (charged ions, hysteresis, etc.) associated with HSQ.

### 8.3.2 Side Gating Effect

One side gated graphene FET was fabricated on the Si face of 4H-SiC (sample 772). The narrowest region of the ribbon is about 60 nm $\times$ 100 nm. The insulating trenches between the narrowest ribbon and the side gates are about 20 nm wide. The ribbon channel and side gates are isolated only by air in the trenches instead of any other dielectric material. The huge ratio ($> 1000$) of length/width of trenches also increases the chances of unexpected connection between the ribbon channel and side gates. For this side gated FET, gate leakage starts at around 3 V for a 60 nm wide trench in a vacuum at 4 K.

A significant side gating effect was observed on this FET at 4 K. Figure 8.8(a) shows that the channel magnetoresistance can be modified by $V_g$. The central resistance peak is due to weak localization. The tiny oscillations at low B field are attributed to universal conductance fluctuations (UCF) that are sensitive to elastic scattering in a sample.

Figure 8.8(b) shows a more clear side gating effect on sample 772. $V_g$ sweeps between

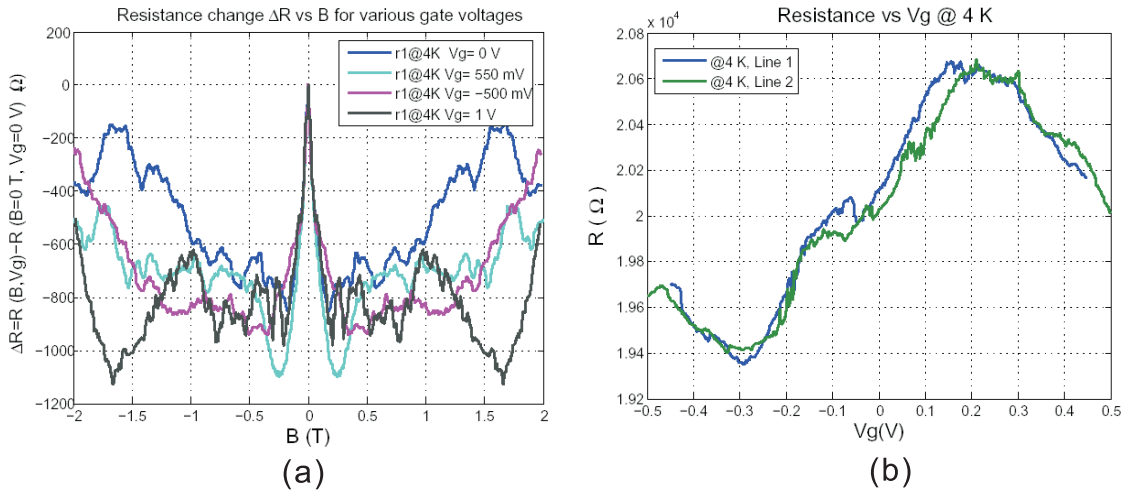


**Figure 8.8:** Side gating effect on a 60nm wide graphene ribbon on th Si face of 4H-SiC (sample 772). (a) Low field magnetoresistance measurement at different $V_g$s at 4 K. (b) Channel resistance as a function of $V_g$. Line 1 and Line 2 show the repeatability of the gating effect.

$\pm$ 0.45 V (Line 1) and between $\pm$ 0.5 V (Line 2), respectively. The resistance curves show similar shapes under these two sweeps, which demonstrate the repeatability of the side gating effect. The total channel resistance is changed about 6 in the whole B sweeping range. However, the nonlinearity of the plots is hard to be explained by the change of carrier number due to the external electric field. One possible explanation is due to the ribbon's rough edges where the edge states are localized. The side gates affect the carrier density along the edges because of the lateral electric field. The complicated scattering of carriers along rough edges could change the whole quantum interference pattern in the sample and and cause the complexity of gating effect. After comparing the MR plots in Figure 8.8(a) and the resistance plot in Figure 8.8(b), we find their resistance fluctuation ranges are close to each other. That indicates that what an external electric field affects For a better side gating effect, it requires a narrower ribbon with smooth edges to open an observable bandgap ($E_g \sim 1/\mathrm{W}$) and a good electric material to fill the trenches to isolate the channel from the side gates.

## *8.4 Summary*

The Dirac properties of carriers in epitaxial graphene has been demonstrated by the Landau level spectroscopy and magnetotransport measurements. These properties include the Berry's phase $\pi$, $\sqrt{B}$ dependence of the Landau level, weak anti-localization, etc. Carriers in epitaxial graphene also show a long phase coherence length and a high mobility. Quantum confinement due to geometry restriction is also observed on a ribbon that is hundreds of nm wide. The electric field effect on epitaxial graphene is realized on both top gated FETs and side gated FETs. All these evidences demonstrate the great potential of epitaxial graphene in future electronic applications.

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